



# H77H2-M4

Rev : A

ECS CONFIDENTIAL

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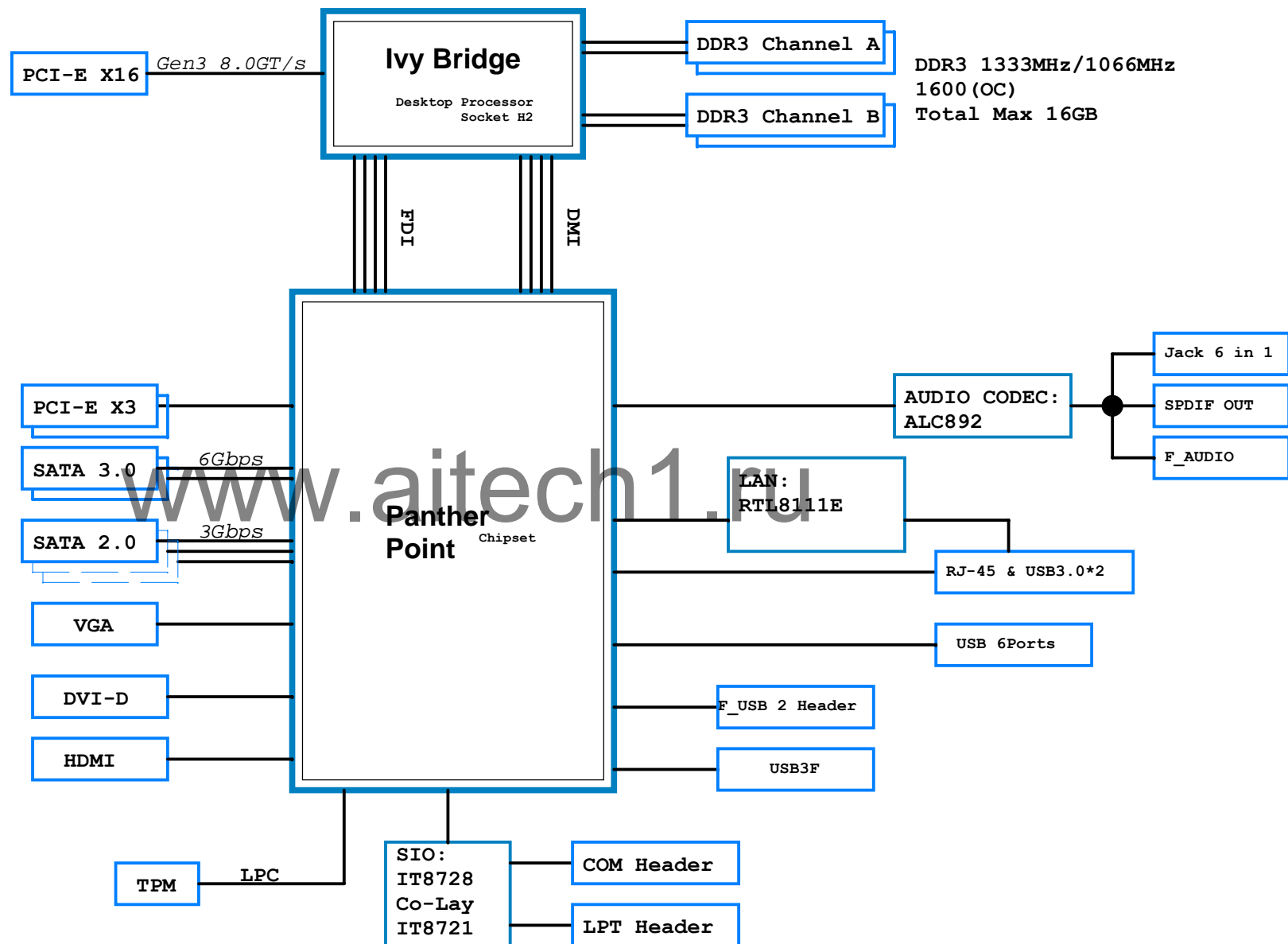
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REVISION HISTORY:

Rev	Date	Notes
VA		Initial version
VA	2011 09 01	page 31 Del LPC DEBUGE HEADER ADD TPM
VA	2011 09 08	page 30 SYS/PWR_FAN 3PIIN&4PIN CO_LAY
VA	2011 09 08	page 24 ADD DP CONNECT
VA	2011 09 08	page 20 ADD PCH DP CONNECT
VA	2011 09 13	page 25 Change USB Rear/Front
V1.0		
V1.0	2011 10 25	page 24 Change hdmi tx0 連線
V1.0	2011 11 28	page 30 Change MC113/MC125/MC126/MC111 TO 10U-16V-08
V1.0	2011 11 28	page 11 Change ER47 TO 75K OHM
V1.0	2011 11 29	page 25 Del CMF9/14/15
V1.0	2011 11 29	page 25 Remove CN2,3,4,5,6,7

- NOTE:
- 1. Model Code: EG7;
  - 2. Modified from H77H2-M4 V:A



PCH-GPIO function

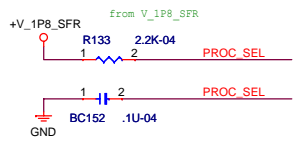
Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

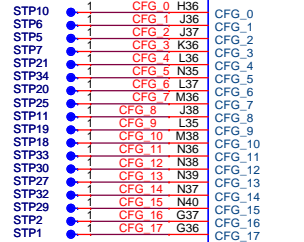
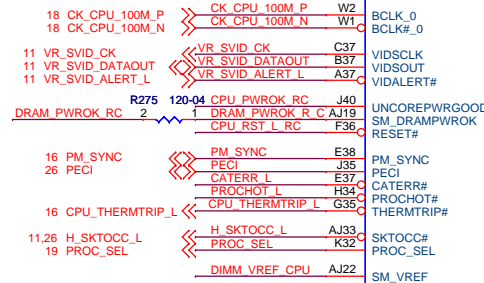
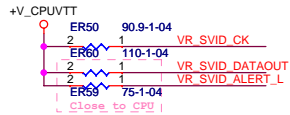
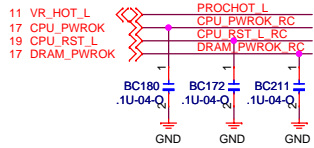
Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
GP26		Over Voltage +V_1P05_PCH	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

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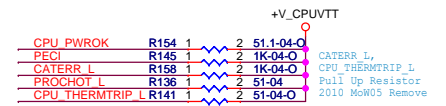
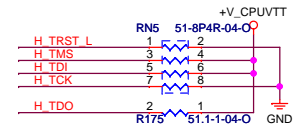
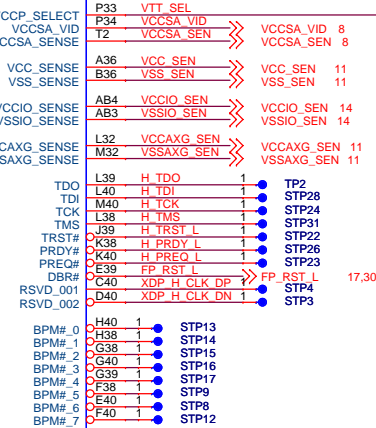




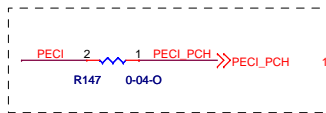
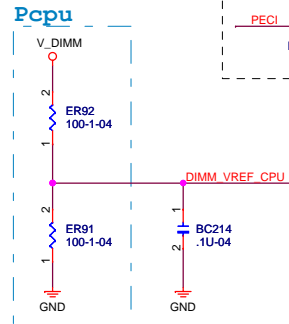
DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



BALLMAP\_REV=1.4



Power Down Sequencing Circuit

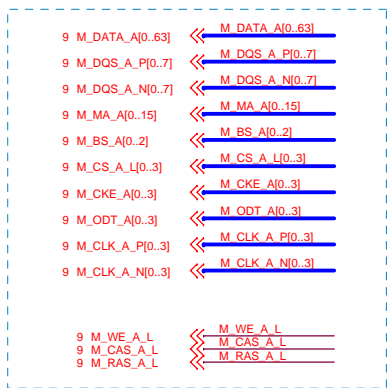


CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

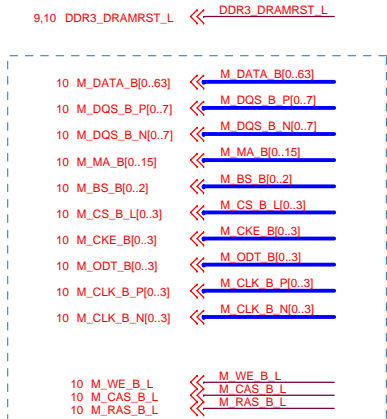
CFG [0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

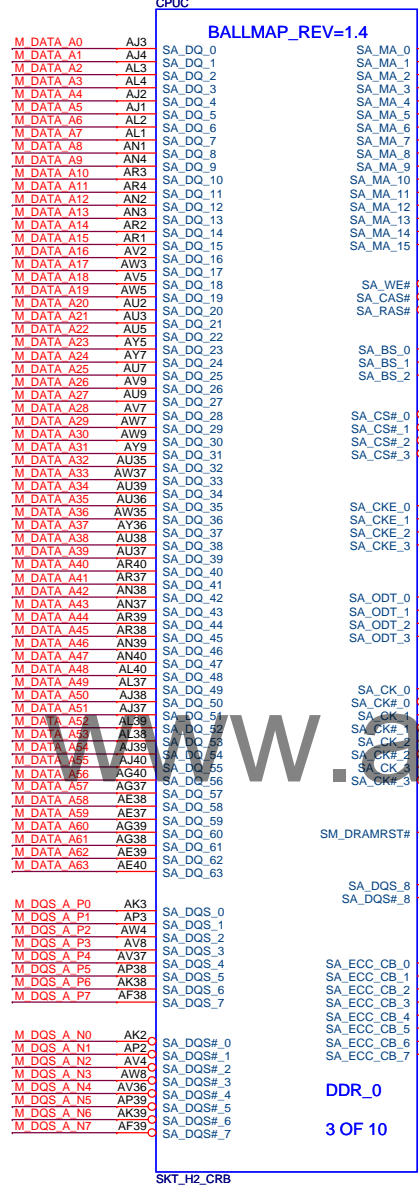
Elitegroup Computer Systems



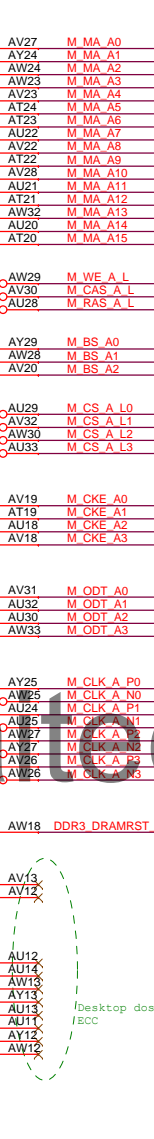
DDR3 CH.A



DDR3 CH.B

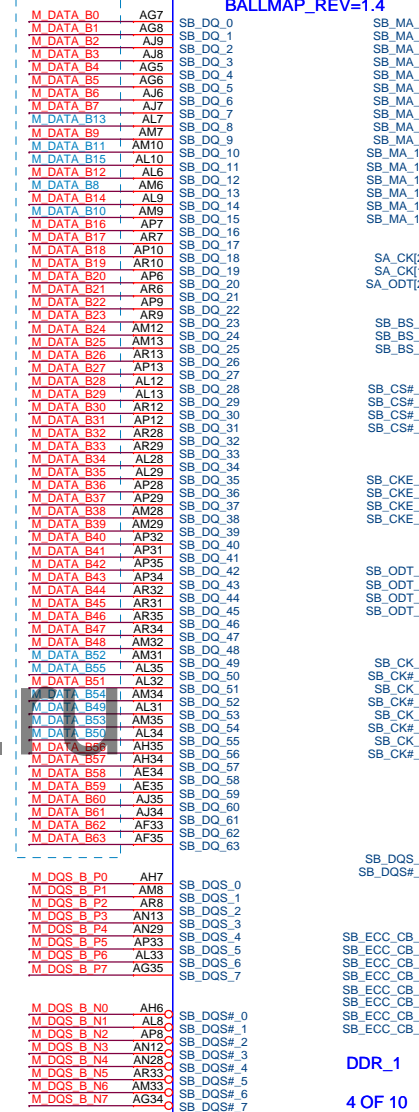


DDR3 CH.A

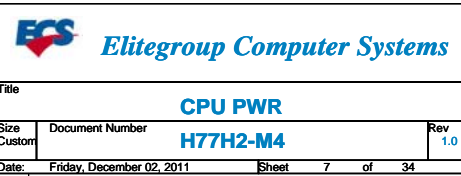


DDR3 CH.A

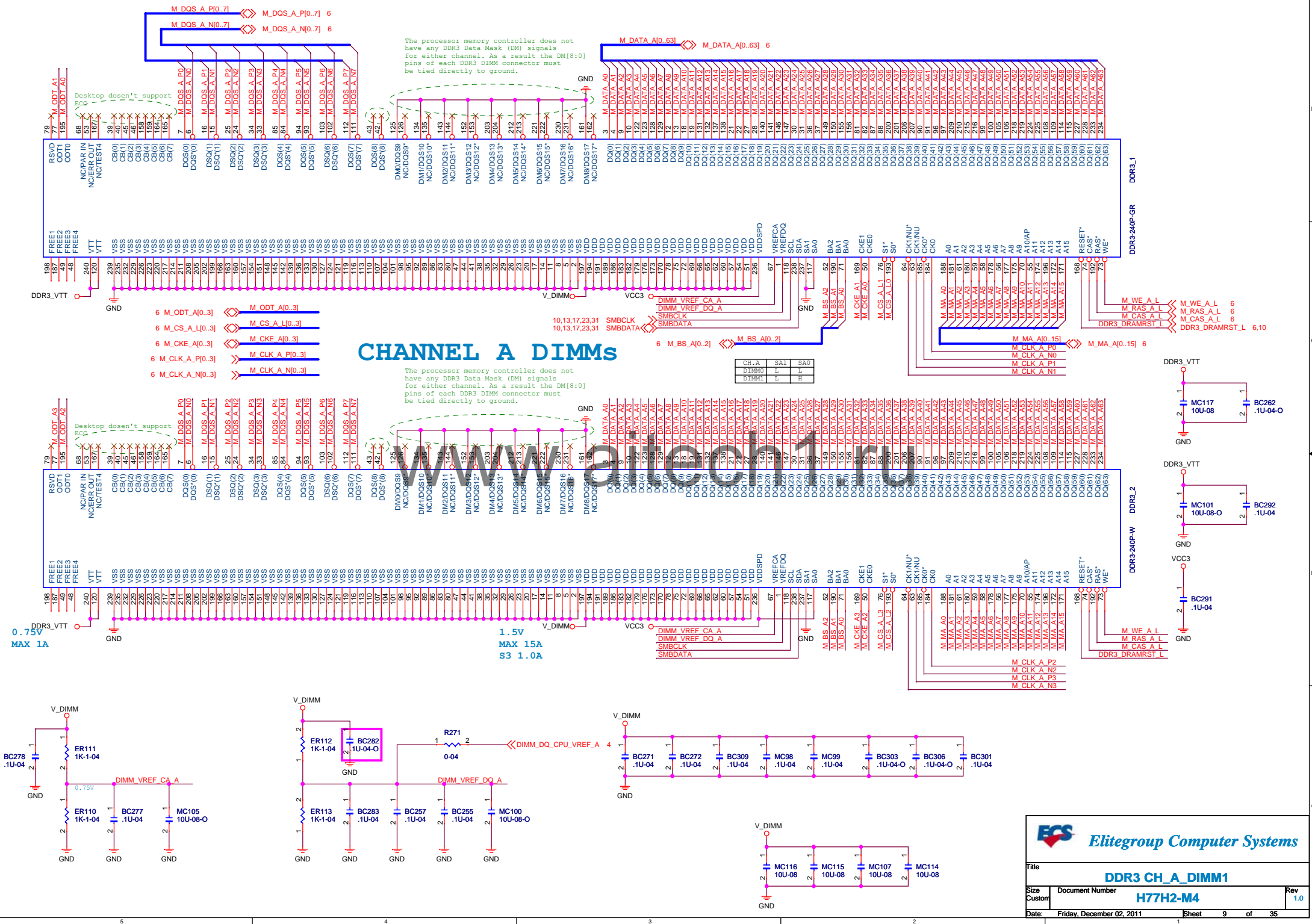
Pay Attention to This Part!



DDR3 CH.B



CPU1			CPU2		
BALLMAP_REV=1.4			BALLMAP_REV=1.4		
A17	VSS_001	AM27	AV11	VSS_181	G8
A23	VSS_002	AM3	AV14	VSS_182	H1
A26	VSS_003	AM30	AV17	VSS_183	H17
A29	VSS_004	AM36	AV3	VSS_184	H2
AA35	VSS_005	AM37	AV35	VSS_185	H20
AA33	VSS_006	AM38	AV38	VSS_186	H23
AA34	VSS_007	AM39	AV6	VSS_187	H26
AA35	VSS_008	AM4	AW10	VSS_188	H29
AA36	VSS_009	AM40	AW11	VSS_189	H33
AA37	VSS_010	AM5	AW14	VSS_190	H35
AA38	VSS_011	AN10	AW16	VSS_191	H37
AA6	VSS_012	AN11	AW36	VSS_192	H39
AB5	VSS_013	AN14	AW6	VSS_193	H5
AC1	VSS_014	AN17	AY11	VSS_194	H6
AC6	VSS_015	AN19	AY14	VSS_195	H9
AD33	VSS_016	AN22	AY18	VSS_196	J11
AD36	VSS_017	AN24	AY35	VSS_197	J17
AD38	VSS_018	AN30	AY4	VSS_198	J20
AD39	VSS_019	AN31	AY6	VSS_199	J23
AD40	VSS_020	AN32	AY8	VSS_200	J26
AD5	VSS_021	AN33	B10	VSS_201	J29
AD8	VSS_022	AN34	B11	VSS_202	J32
AE3	VSS_023	AN35	B17	VSS_203	K1
AE33	VSS_024	AN36	B23	VSS_204	K12
AE36	VSS_025	AN5	B29	VSS_205	K13
AF1	VSS_026	AN6	B35	VSS_206	K14
AF34	VSS_027	AN8	B38	VSS_207	K17
AF36	VSS_028	AN9	B6	VSS_208	K2
AF37	VSS_029	AP1	C11	VSS_209	K23
AF40	VSS_030	AP11	C12	VSS_210	K26
AF5	VSS_031	AP14	C17	VSS_211	K29
AF6	VSS_032	AP17	C20	VSS_212	K33
AG36	VSS_033	AP22	C23	VSS_213	K35
AH2	VSS_034	AP25	C26	VSS_214	K37
AH3	VSS_035	AP27	C29	VSS_215	K39
AH33	VSS_036	AP30	C32	VSS_216	K5
AH37	VSS_037	AP36	C35	VSS_217	K6
AH38	VSS_038	AP37	C7	VSS_218	L10
AH39	VSS_039	AP4	C8	VSS_219	L17
AH40	VSS_040	AP40	D17	VSS_220	L20
AH5	VSS_041	AP5	D2	VSS_221	L23
AH8	VSS_042	AR11	D20	VSS_222	L26
AJ12	VSS_043	AR14	D23	VSS_223	L29
AJ15	VSS_044	AR17	D26	VSS_224	M1
AJ18	VSS_045	AR18	D29	VSS_225	M17
AJ21	VSS_046	AR19	D32	VSS_226	M20
AJ25	VSS_047	AR27	D37	VSS_227	M23
AJ5	VSS_048	AR30	E12	VSS_228	M26
AJ36	VSS_049	AR36	E17	VSS_229	M3
AJ27	VSS_050	AT1	E20	VSS_230	M35
AK1	VSS_051	AT10	E23	VSS_231	M37
AK10	VSS_052	AT12	E26	VSS_232	M39
AK13	VSS_053	AT13	E29	VSS_233	M5
AK14	VSS_054	AT15	E32	VSS_234	M6
AK16	VSS_055	AT16	E36	VSS_235	M9
AK22	VSS_056	AT17	E7	VSS_236	M33
AK28	VSS_057	AT2	E8	VSS_237	M38
AK31	VSS_058	AT25	F1	VSS_238	P40
AK32	VSS_059	AT27	F10	VSS_239	P5
AK33	VSS_060	AT28	F13	VSS_240	P6
AK34	VSS_061	AT29	F14	VSS_241	P36
AK35	VSS_062	AT3	F17	VSS_242	P38
AK36	VSS_063	AT30	F2	VSS_243	P39
AK37	VSS_064	AT31	F20	VSS_244	R8
AK4	VSS_065	AT32	F23	VSS_245	T1
AK40	VSS_066	AT33	F26	VSS_246	T5
AK5	VSS_067	AT34	F29	VSS_247	T6
AK6	VSS_068	AT35	F35	VSS_248	T8
AK7	VSS_069	AT36	F37	VSS_249	V1
AK8	VSS_070	AT38	F39	VSS_250	V2
AK9	VSS_071	AT39	F5	VSS_251	V3
AL11	VSS_072	AT4	F6	VSS_252	V34
AL14	VSS_073	AT40	F9	VSS_253	V35
AL17	VSS_074	AT5	G11	VSS_254	V36
AL19	VSS_075	AT6	G12	VSS_255	V37
AL24	VSS_076	AT7	G17	VSS_256	V38
AL27	VSS_077	AT8	G20	VSS_257	V39
AL30	VSS_078	AT9	G23	VSS_258	V40
AL36	VSS_079	AT15	G26	VSS_259	V5
AL5	VSS_080	AT16	G29	VSS_260	W6
AM1	VSS_081	AT17	G34	VSS_261	Y5
AM11	VSS_082	AT18	G7	VSS_262	Y8
AM14	VSS_083	AT19	AY37	VSS_263	
AM17	VSS_084	AT20	B3	VSS_264	
AM2	VSS_085	AT21		VSS_265	
AM21	VSS_086	AT22		VSS_266	
AM23	VSS_087	AT23		VSS_267	
AM25	VSS_088	AT24		VSS_268	
	VSS_089	AT25		VSS_269	
	VSS_090	AT26		VSS_270	
		AT27		VSS_271	
		AT28		VSS_272	
		AT29		VSS_273	
		AT30		VSS_274	
		AT31		VSS_275	
		AT32		VSS_276	
		AT33		VSS_277	
		AT34		VSS_278	
		AT35		VSS_279	
		AT36		VSS_280	
		AT37		VSS_281	
		AT38		VSS_282	
		AT39		VSS_283	
		AT40		VSS_284	
		AT41		VSS_285	
		AT42		VSS_286	
		AT43		VSS_287	
		AT44		VSS_288	
		AT45		VSS_289	
		AT46		VSS_290	
		AT47		VSS_291	
		AT48		VSS_292	
		AT49		VSS_293	
		AT50		VSS_294	
		AT51		VSS_295	
		AT52		VSS_296	
		AT53		VSS_297	
		AT54		VSS_298	
		AT55		VSS_299	
		AT56		VSS_300	
		AT57		VSS_301	
		AT58		VSS_302	
		AT59		VSS_303	
		AT60		VSS_304	
		AT61		VSS_305	
		AT62		VSS_306	
		AT63		VSS_307	
		AT64		VSS_308	
		AT65		VSS_309	
		AT66		VSS_310	
		AT67		VSS_311	
		AT68		VSS_312	
		AT69		VSS_313	
		AT70		VSS_314	
		AT71		VSS_315	
		AT72		VSS_316	
		AT73		VSS_317	
		AT74		VSS_318	
		AT75		VSS_319	
		AT76		VSS_320	
		AT77		VSS_321	
		AT78		VSS_322	
		AT79		VSS_323	
		AT80		VSS_324	
		AT81		VSS_325	
		AT82		VSS_326	
		AT83		VSS_327	
		AT84		VSS_328	
		AT85		VSS_329	
		AT86		VSS_330	
		AT87		VSS_331	
		AT88		VSS_332	
		AT89		VSS_333	
		AT90		VSS_334	
		AT91		VSS_335	
		AT92		VSS_336	
		AT93		VSS_337	
		AT94		VSS_338	
		AT95		VSS_339	
		AT96		VSS_340	
		AT97		VSS_341	
		AT98		VSS_342	
		AT99		VSS_343	
		AT100		VSS_344	
		AT101		VSS_345	
		AT102		VSS_346	
		AT103		VSS_347	
		AT104		VSS_348	
		AT105		VSS_349	
		AT106		VSS_350	
		AT107		VSS_351	
		AT108		VSS_352	
		AT109		VSS_353	
		AT110		VSS_354	
		AT111		VSS_355	
		AT112		VSS_356	
		AT113		VSS_357	
		AT114		VSS_358	
		AT115		VSS_359	
		AT116		VSS_360	
		AT117			
		AT118			
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		AT228			
		AT229			



# CHANNEL A DIMMs

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

CH_A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

Title  
**DDR3 CH\_A\_DIMM1**

Size  
Customer

Document Number  
**H77H2-M4**

Rev  
**1.0**

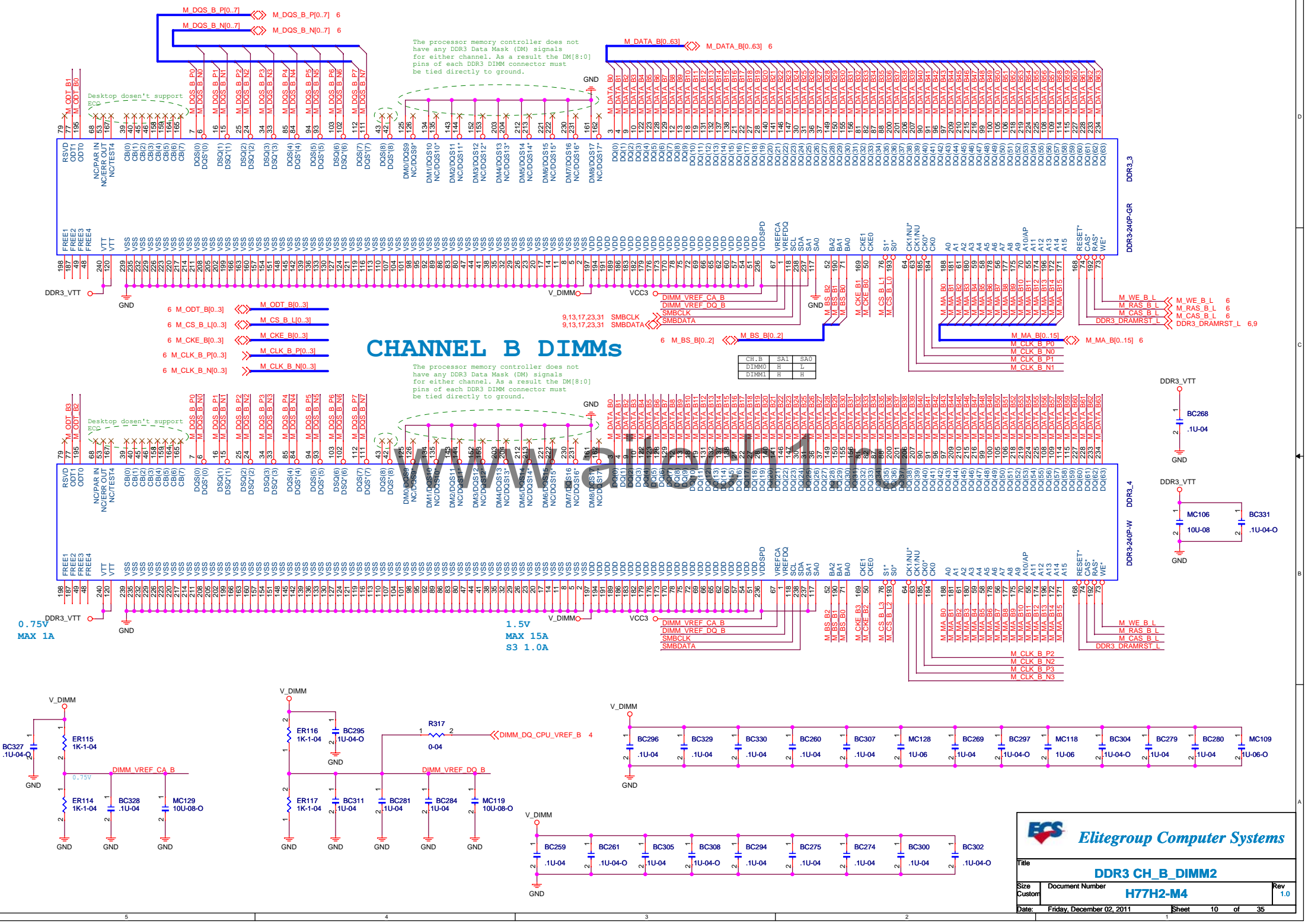
Date: Friday, December 02, 2011

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The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

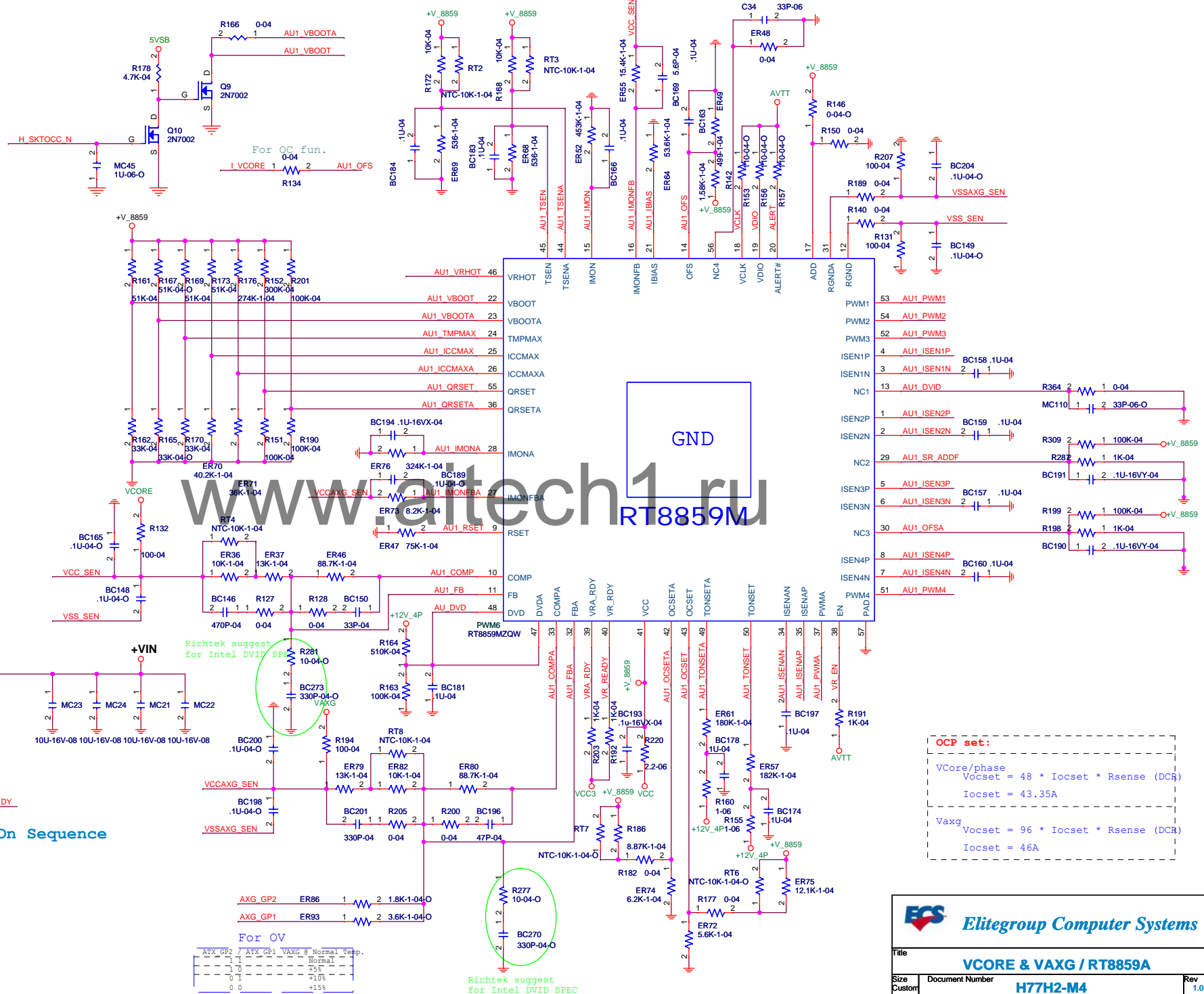
The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

## CHANNEL B DIMMs



## External Connection

Pin	Signal	Pin	Signal
	VCC		VCC
	+V_CPUVTT		AVTT
	+12V_4P		+12V_4P
	VCC3		VCC3
	+VIN		+VIN
	+VSB		+VSB
5	VR_EN	VR_EN	VR_EN
5	VR_SVID_ALERT_L	ALERT	VR_SVID_ALERT_L
5	VR_SVID_DATA_OUT	VDBIO	VR_SVID_DATA_OUT
5	VR_SVID_CLK	VCLK	VR_SVID_CLK
5	VR_HOT_L	AU1_VRHOT	VR_HOT_L
12	AU1_PWM[1..4]	AU1_PWM[1..4]	AU1_PWM[1..4]
12	AU1_ISEN1P	AU1_ISEN1P	AU1_ISEN1P
12	AU1_ISEN1N	AU1_ISEN1N	AU1_ISEN1N
12	AU1_ISEN2P	AU1_ISEN2P	AU1_ISEN2P
12	AU1_ISEN2N	AU1_ISEN2N	AU1_ISEN2N
12	AU1_ISEN3P	AU1_ISEN3P	AU1_ISEN3P
12	AU1_ISEN3N	AU1_ISEN3N	AU1_ISEN3N
12	AU1_ISEN4P	AU1_ISEN4P	AU1_ISEN4P
12	AU1_ISEN4N	AU1_ISEN4N	AU1_ISEN4N
5	VCC_SEN	VCC_SEN	VCC_SEN
5	VSS_SEN	VSS_SEN	VSS_SEN
5,17	VR_READY	VR_READY	VR_READY
12	AU1_PWMMA	AU1_PWMMA	AU1_PWMMA
12	AU1_ISENAP	AU1_ISENAP	AU1_ISENAP
12	AU1_ISENAN	AU1_ISENAN	AU1_ISENAN
5	VCCA_XG_SEN	VCCA_XG_SEN	VCCA_XG_SEN
5	VSSA_XG_SEN	VSSA_XG_SEN	VSSA_XG_SEN
26	AXG_GP1	AXG_GP1	AXG_GP1
26	AXG_GP2	AXG_GP2	AXG_GP2
13	I_VCORE	I_VCORE	I_VCORE
5,26	H_SKTOCC_L	H_SKTOCC_N	H_SKTOCC_L



## External Connection



11 AU1\_PWM[1..4] AU1\_PWM[1..4]

11 AU1\_ISEN1P AU1\_ISEN1P

11 AU1\_ISEN1N AU1\_ISEN1N

11 AU1\_ISEN2P AU1\_ISEN2P

11 AU1\_ISEN2N AU1\_ISEN2N

11 AU1\_ISEN3P AU1\_ISEN3P

11 AU1\_ISEN3N AU1\_ISEN3N

11 AU1\_ISEN4P AU1\_ISEN4P

11 AU1\_ISEN4N AU1\_ISEN4N

5,11 VCC\_SEN VCC\_SEN

5,11 VSS\_SEN VSS\_SEN

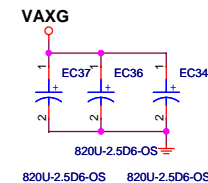
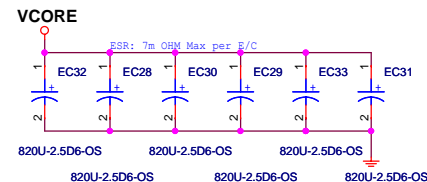
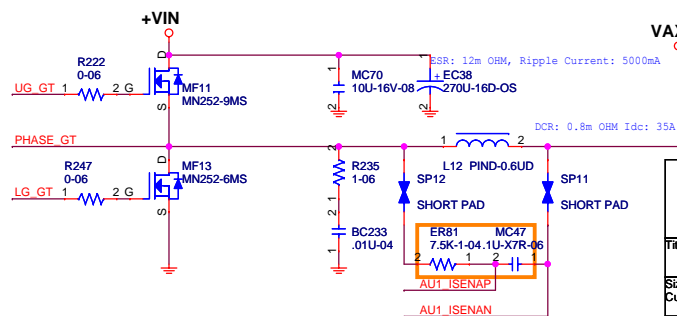
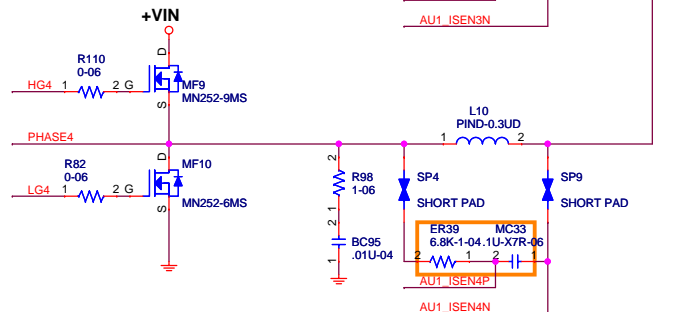
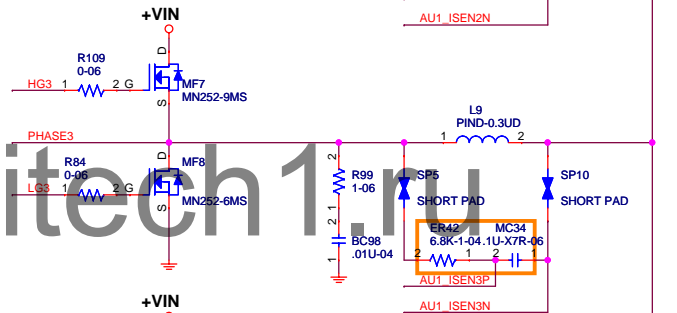
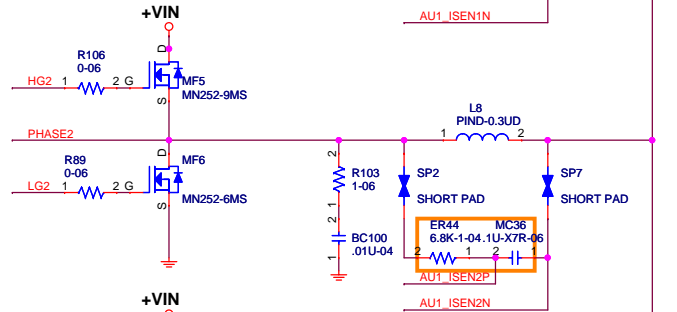
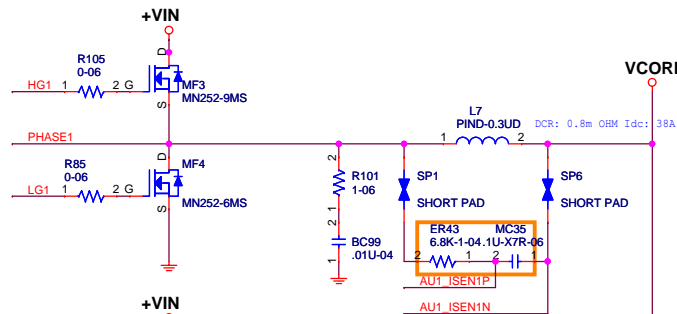
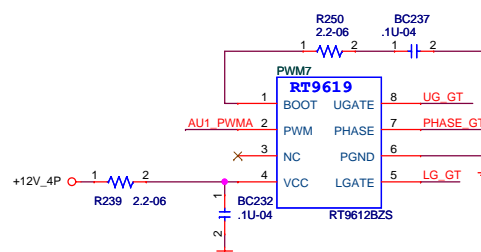
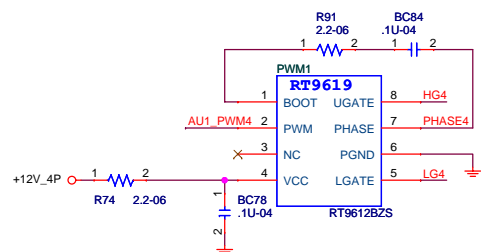
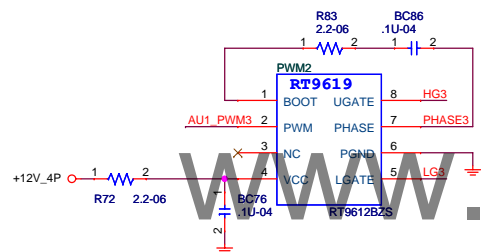
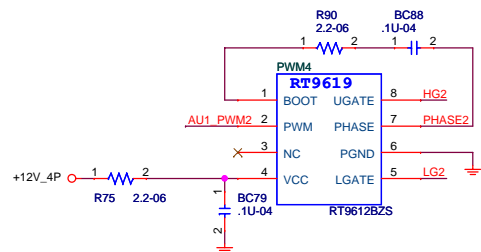
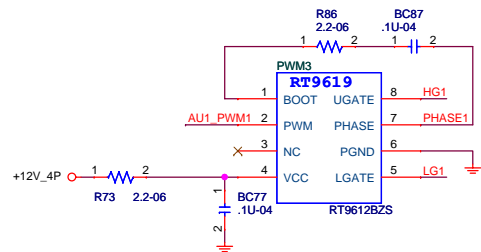
11 AU1\_PWMA AU1\_PWMA

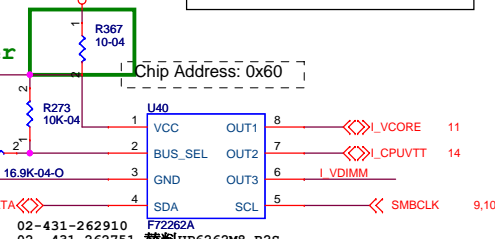
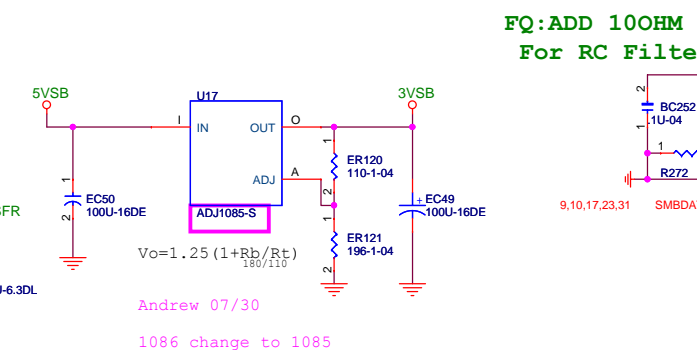
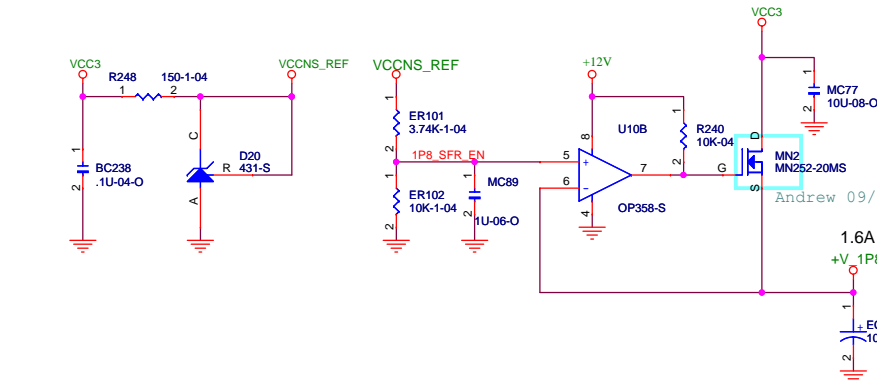
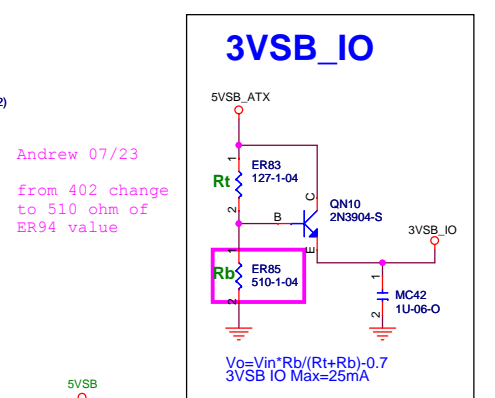
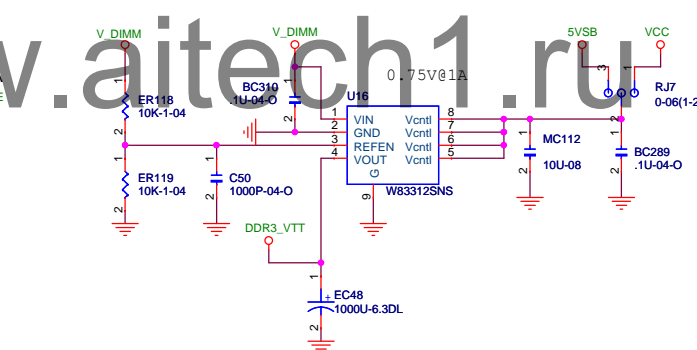
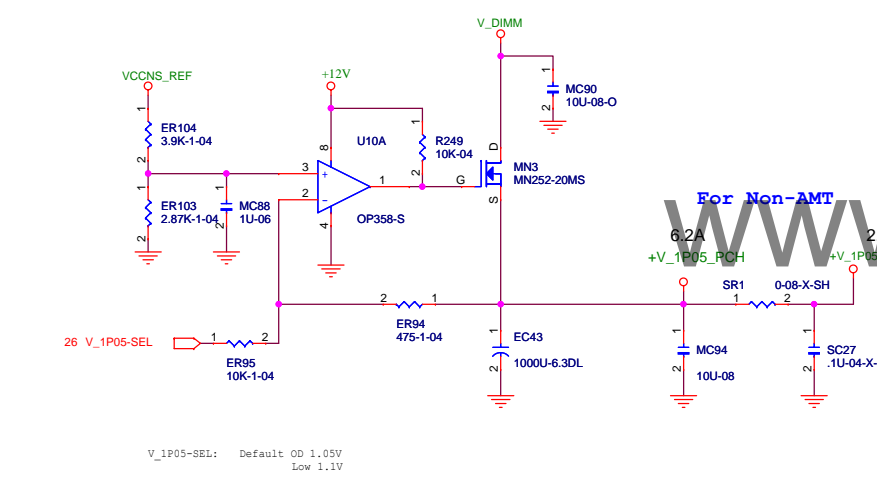
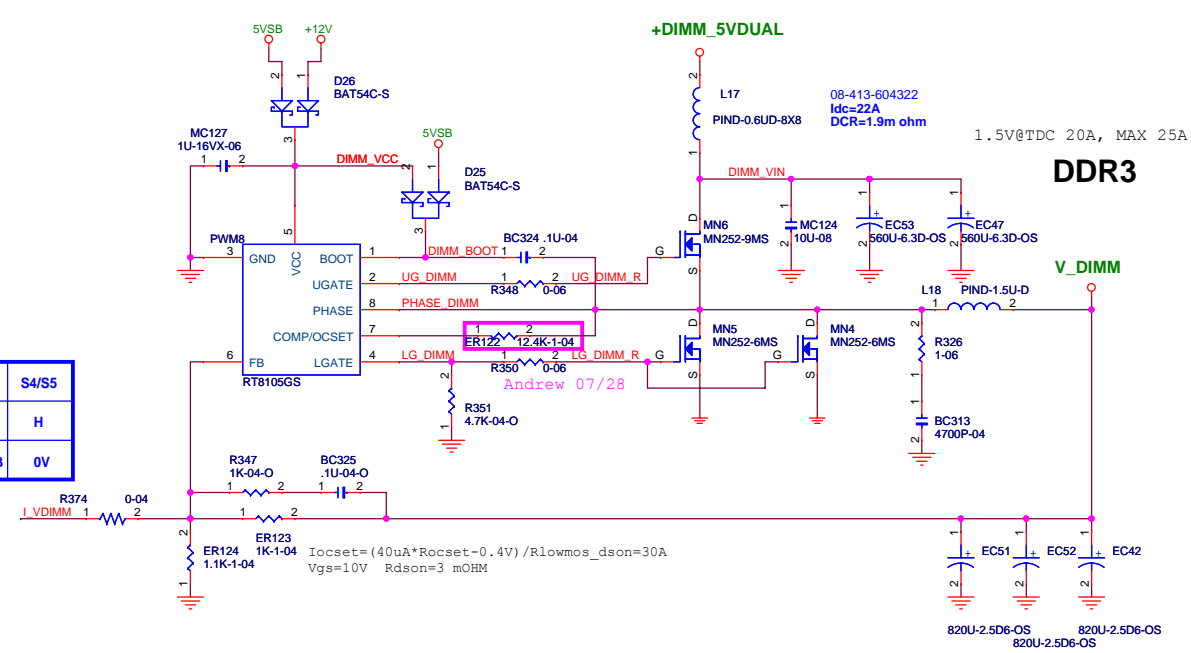
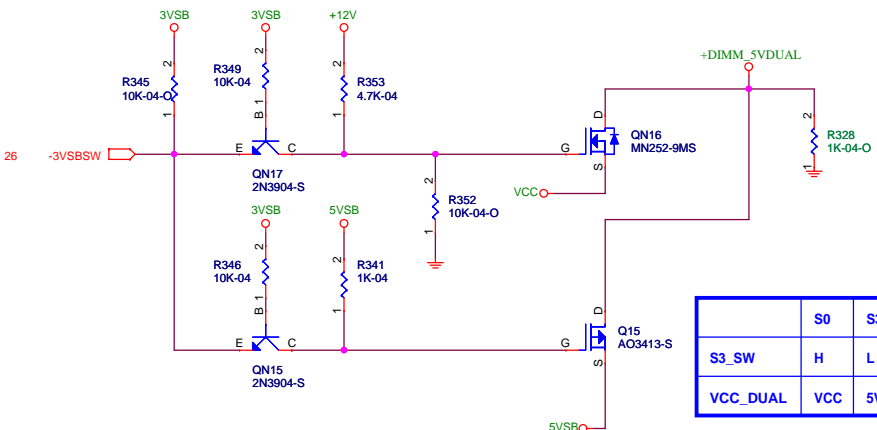
11 AU1\_ISENAP AU1\_ISENAP

11 AU1\_ISENAN AU1\_ISENAN

5,11 VCCAXG\_SEN VCCAXG\_SEN

5,11 VSSAXG\_SEN VSSAXG\_SEN

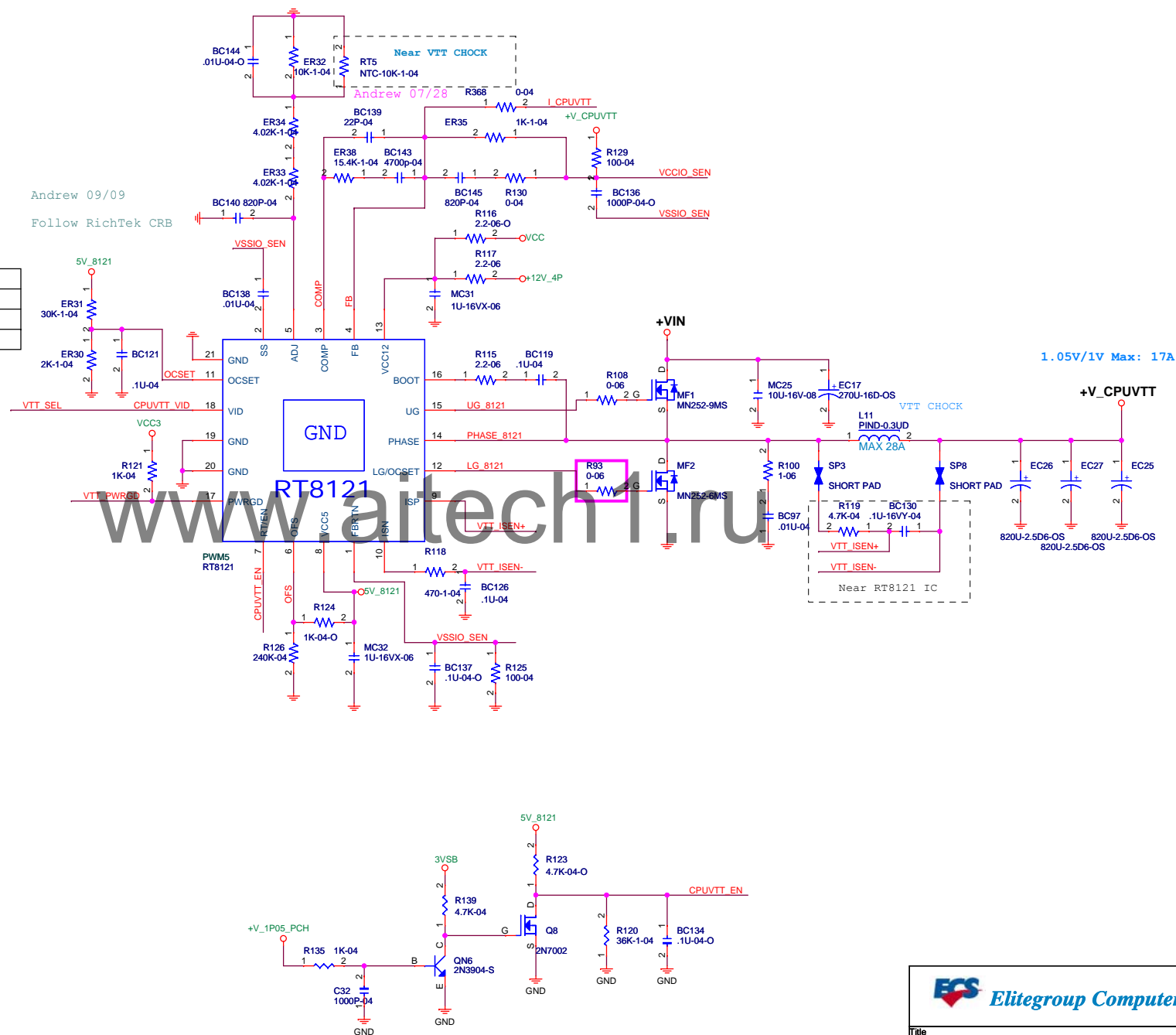




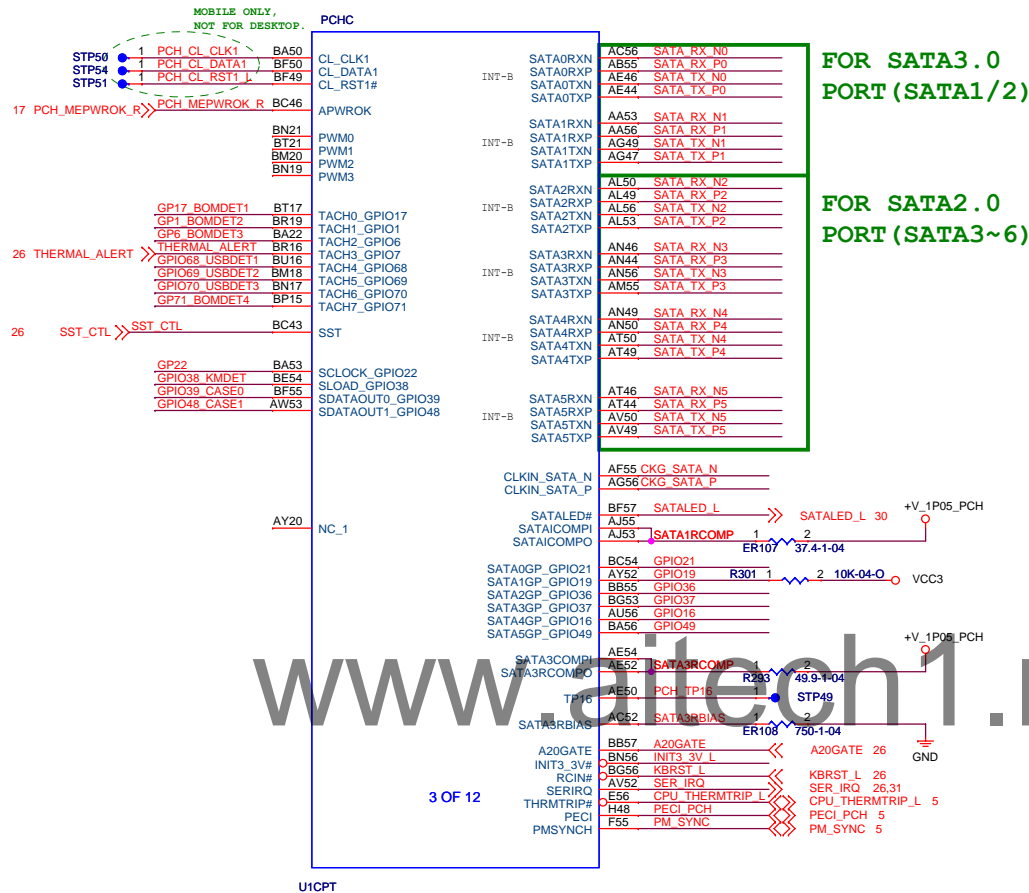
Pin-to-pin comparison diagram for VCC, VDD, and VDDQ pins. The diagram shows two columns of pins with their corresponding functions and connections. The left column lists pins for a device, and the right column lists pins for another device. Connections are indicated by lines between the pins.

Pin	Function	Pin	Function
VCC		VCC	
+12V_4P		+12V_4P	
3V5B		3V5B	
5V5B		5V5B	
+V_1P05_PCH		+V_1P05_PCH	
+V_CPUVTT		+V_CPUVTT	
VTT_SEL		VTT_SEL	
VTT_PWGRD		VTT_PWGRD	
VCCIO_SEN		VCCIO_SEN	
VSSIO_SEN		VSSIO_SEN	
I_CPUVTT		I_CPUVTT	

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



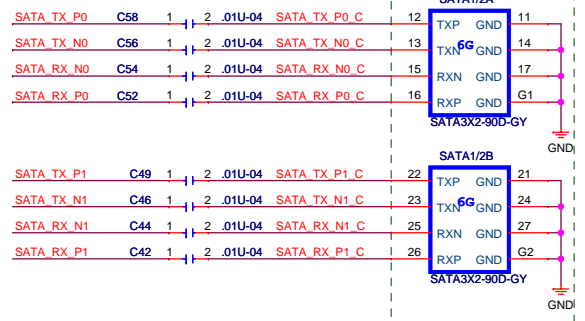




FOR SATA3.0  
PORT (SATA1/2)

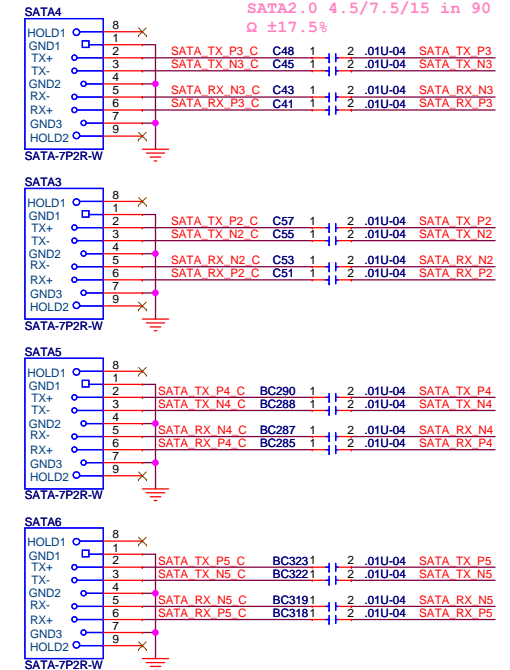
FOR SATA2.0  
PORT (SATA3~6)

## SATA3.0



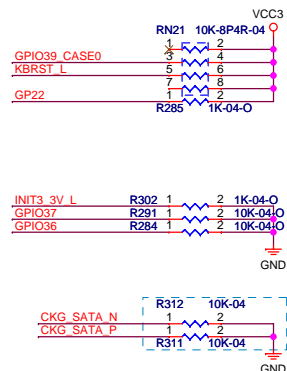
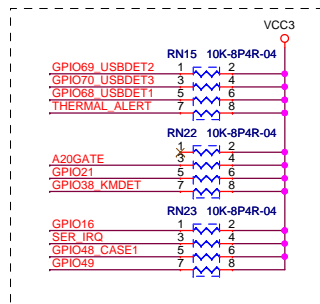
## SATA2.0

Layout Note:  
SATA3.0 4.5/7.5/20 in 85  
Q ±17.5%  
SATA2.0 4.5/7.5/15 in 90  
Q ±17.5%



	SYS/PWR_FAN 3PIN	SYS/PWR_FAN 4PIN
SP17_BOMDET1	high	low
SP1_BOMDET2	high	low

Default GPI set to Pull Up:



1 為GALAN, 0 為100Mlan

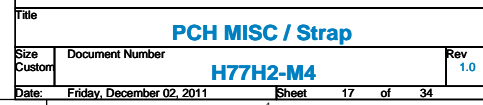
Stuff for  
Integrated Clock Mode

	SYS/PWR_FAN 3PIN	SYS/PWR_FAN 4PIN
GP17_BOMDET1	high	low
GP1_BOMDET2	high	low

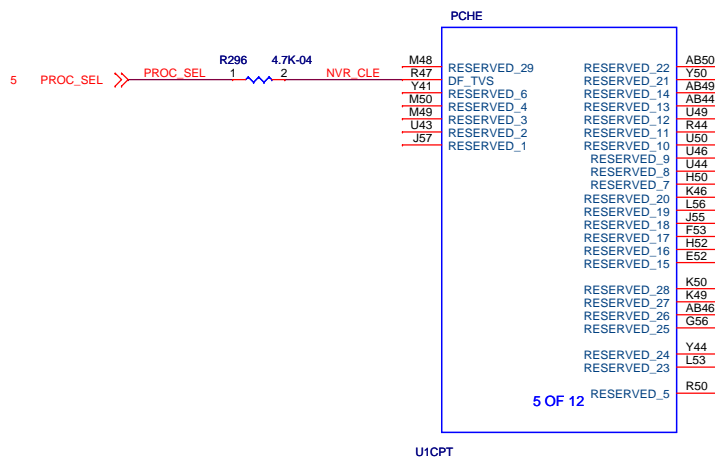


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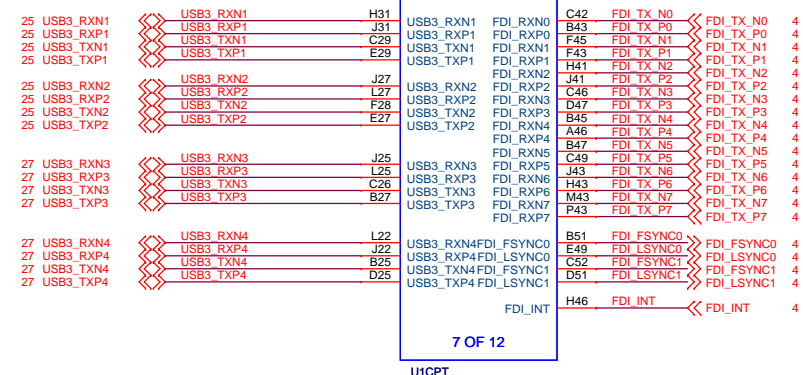




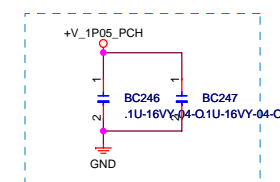


USB3F

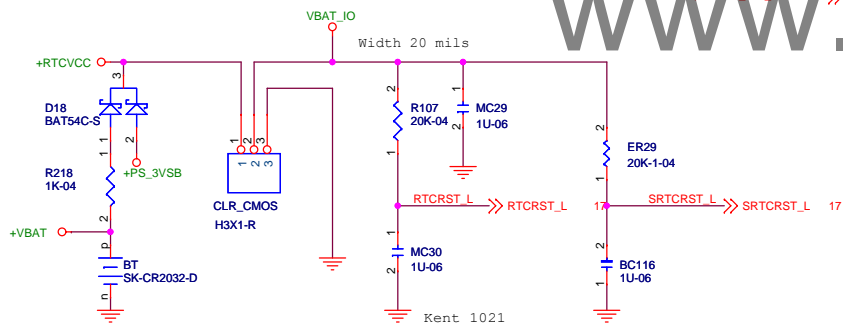
USB3LAN



STITCHING CAP FOR FDI.



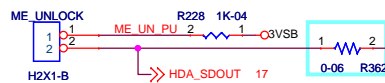
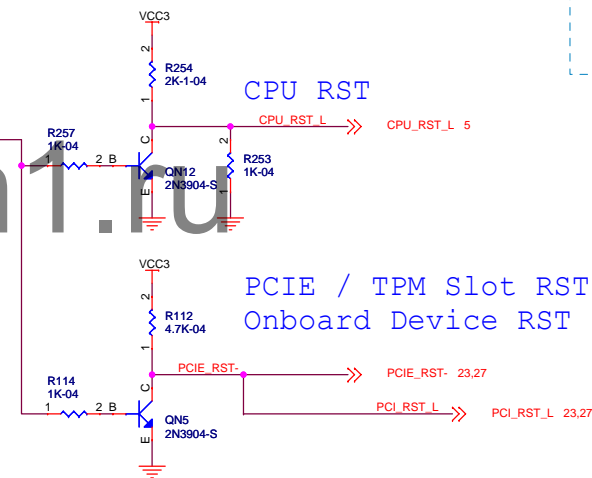
CLR\_CMOS



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CPU RST

PCIE / TPM Slot RST / Onboard Device RST



ME Enable/Disable

	ME_UNLOCK
1-2	UNLOCK
Float	LOCK

Andrew 08/02

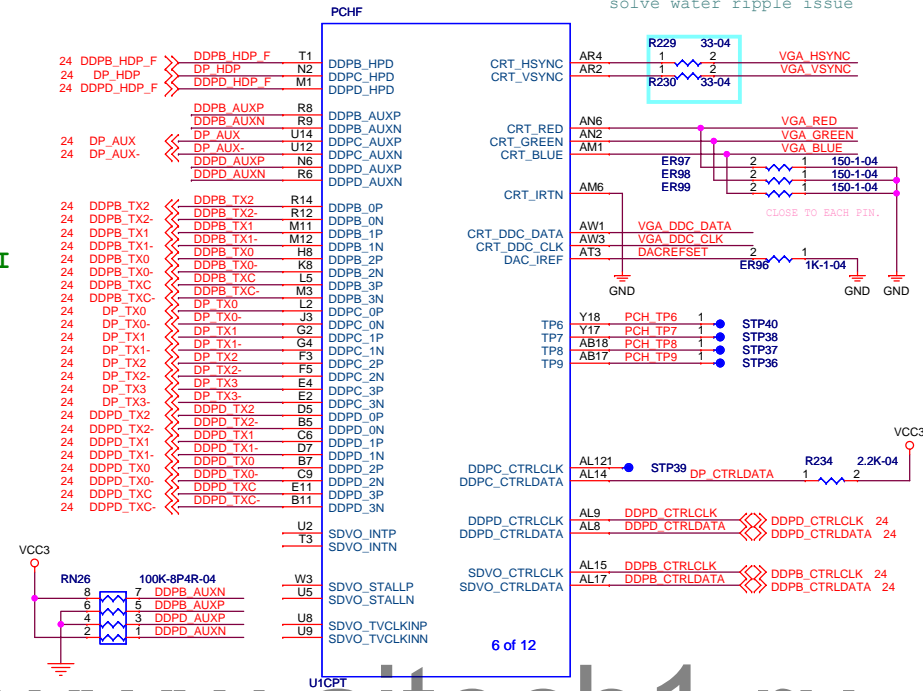
Modify ME\_UNLOCK from vendor

solve water ripple issue

HDMI

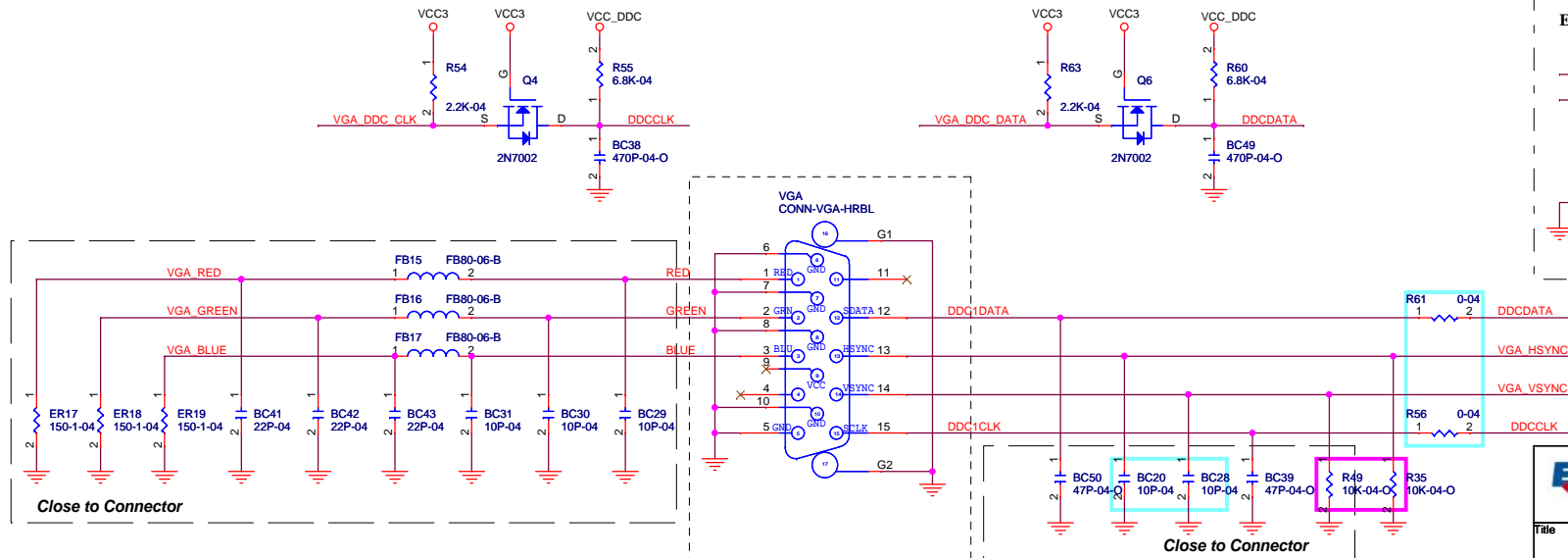
DP

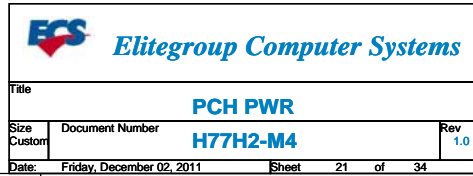
DVI

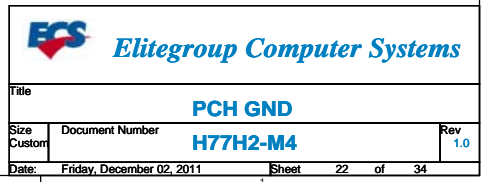


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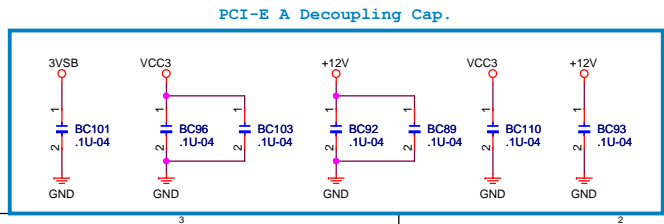
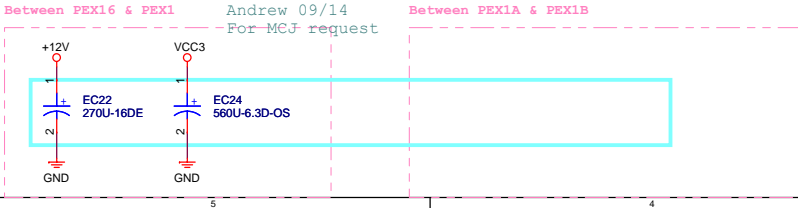
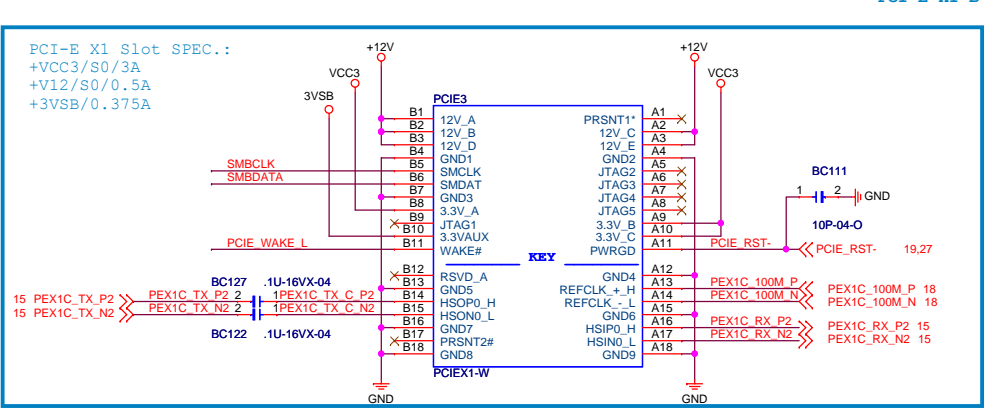
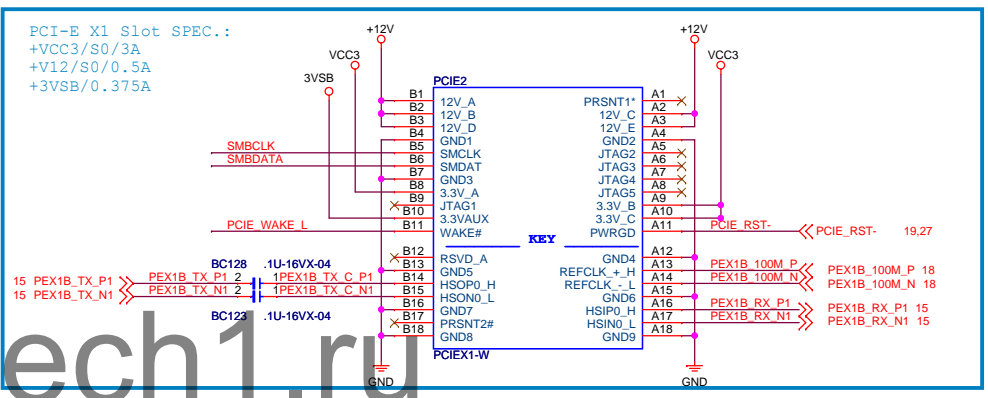
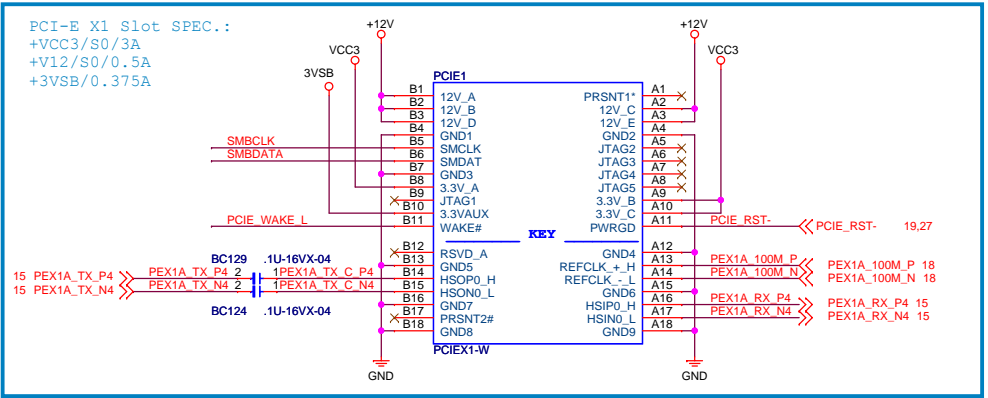
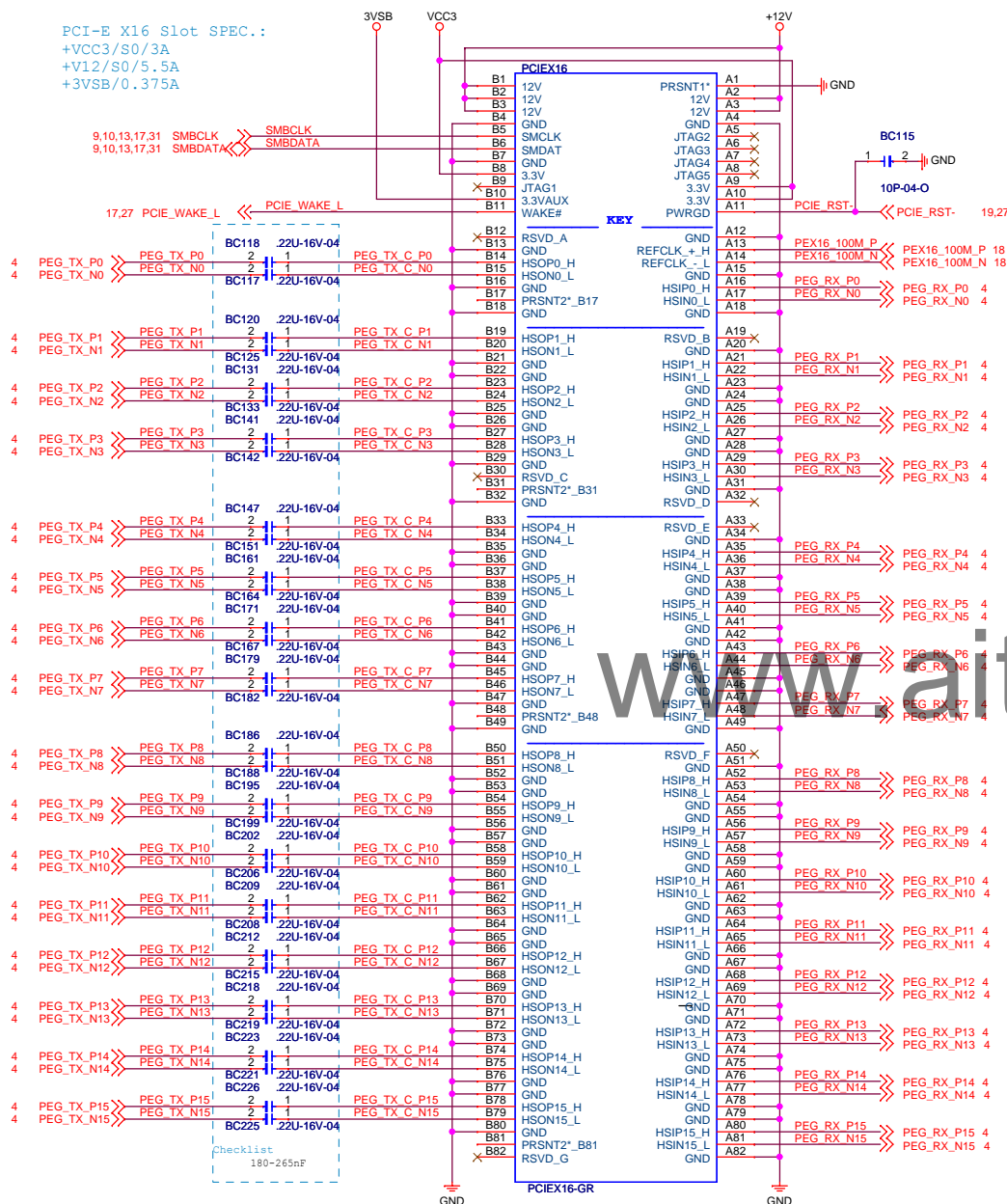
## VGA CONNECT







PCI-E X16 Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A



Elitegroup Computer Systems	
Slot PCI-EX16 / PCI-EX1	
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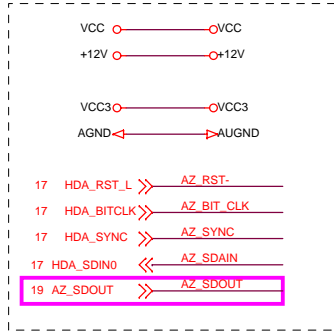




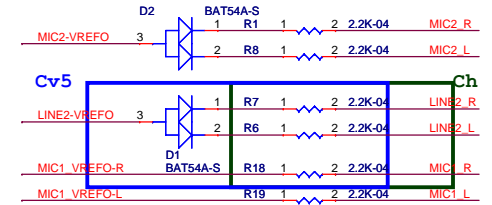
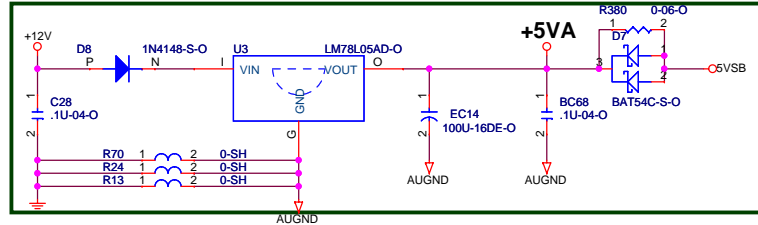




## External Connection

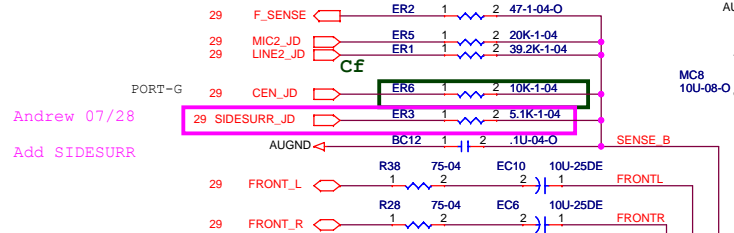


## Cv3



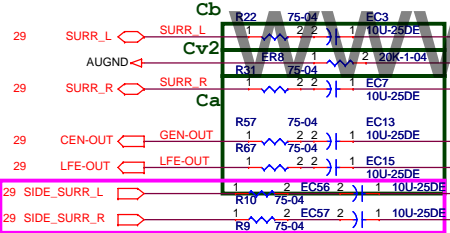
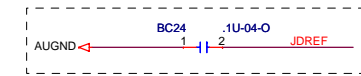
## Cv5

## Ch



Andrew 07/28

Add SIDESURR



Andrew 07/28

Add Side-Surround

## BOM Difference

Location	ALC892 7.1CH	VT1818S 5.1CH	VT1828S 7.1CH	VT1705B 5.1CH	VT1705B 7.1CH	ALC662 5.1CH
Ca	V	X	V	X	V	X
Cb	V	X	V	X	V	X
Cc	ALC892	VT1818S	VT1828S	VT1705BS	VT1705BS	ALC662-VC-GR
Cd	V	X	V	X	V	X
Ce	AUDIO-26P	AUDIO-3P-HDA near HS	AUDIO-26P	AUDIO-3P-HDA near HS	AUDIO-26P	AUDIO-3P-HDA near HS
Cf	V	X	V	X	V	X
Cg	V	X	V	X	V	X
Ch	2.2K-04	3.3K-04	3.3K-04	3.3K-04	3.3K-04	2.2K-04
Cv1	V	X	V	X	V	X
Cv2	20K-1-04	5.1K-1-04	5.1K-1-04	5.1K-1-04	5.1K-1-04	20K-1-04
Cv3	X	V	V	V	V	V
Cv4	V	X	X	X	X	X
Cv5	V	V	V	V	V	X
Cv6	X	V	V	V	V	V

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

Pin2  
VT1705: GPIO(\*)/SPDIFO  
VT1818: GPIO(\*)/SPDIFO/D-MIC\_C  
ALC892: GPIO(\*)/SPDIFO/D-MIC\_C

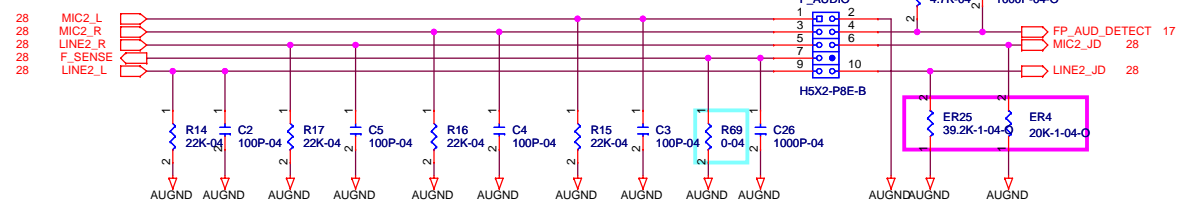
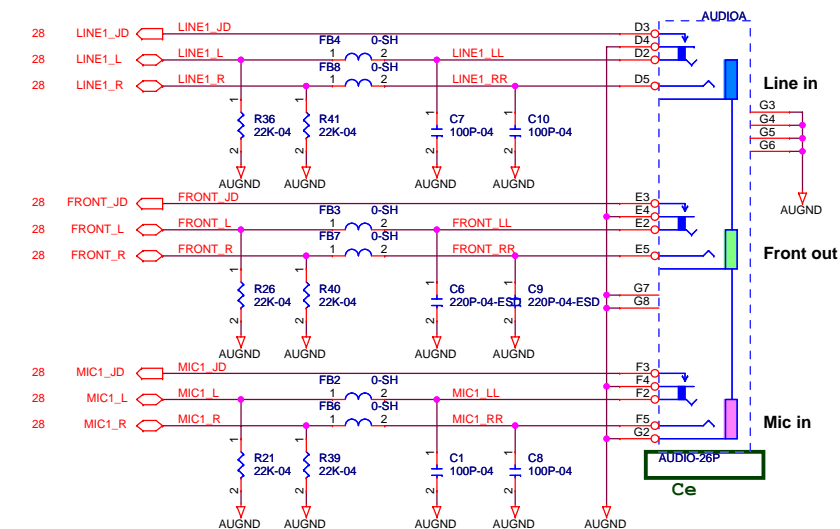
Pin3  
VT1705: GPIO  
VT1818: GPIO(\*)/D-MIC\_D  
ALC892: REGREF

Pin4  
VT1705: D-GND  
VT1818: D-GND  
ALC892: GPIO(\*)/D-MIC\_D

<b>AUDIO CODEC</b>	
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Size Custom	<b>H77H2-M4</b>
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## REAR-AUDIO

## FRONT-AUDIO

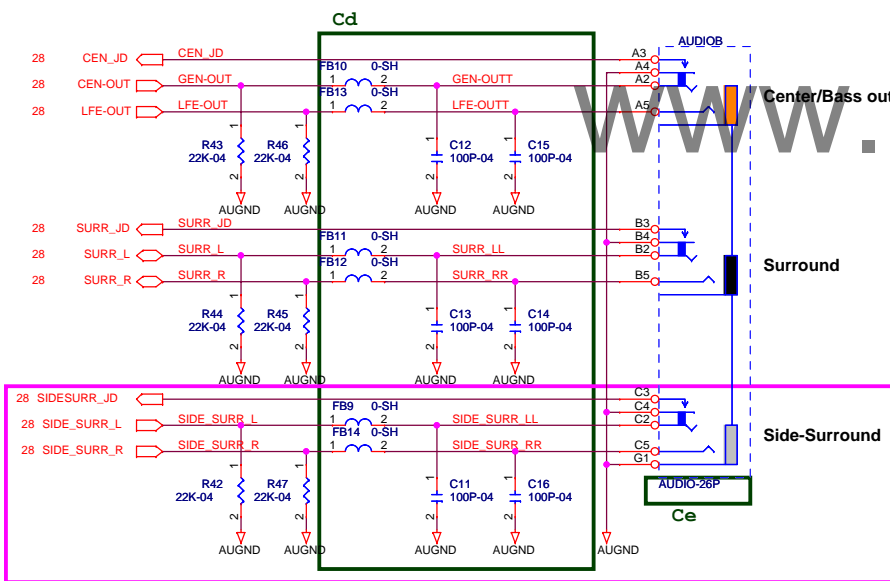
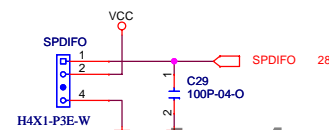


Andrew 09/01

Stuff R69

Line-out ( speak out) 的對地電容改成 for ESD的VPORT 電容 04-140-221005

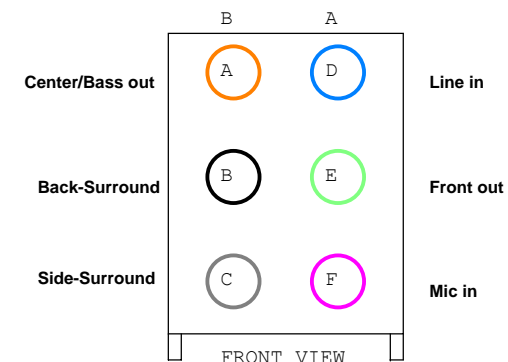
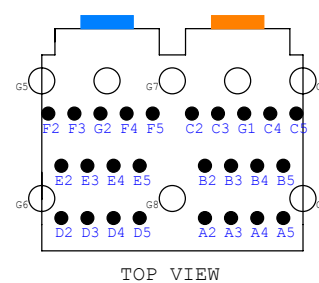
## SPDIF-OUT



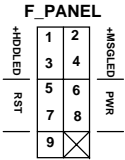
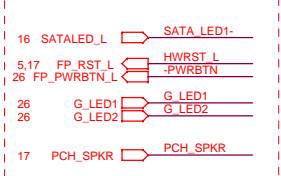
Andrew 07/28

Change to Side-Surround

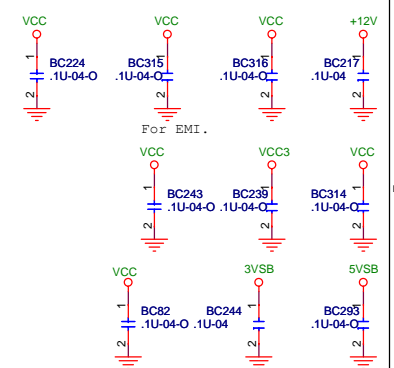
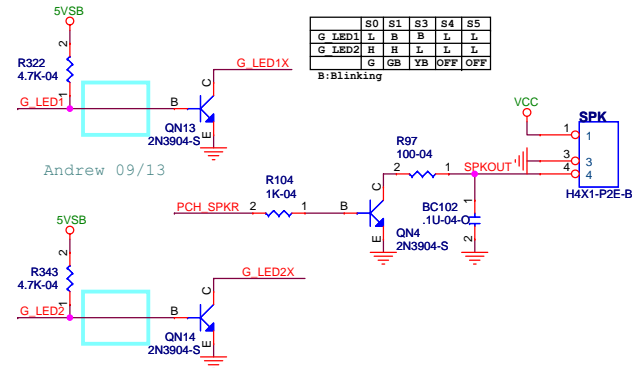
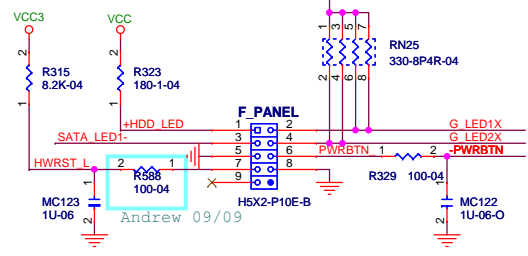
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External Connection

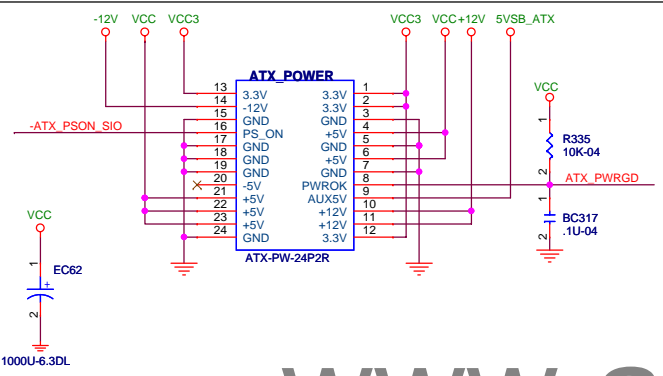
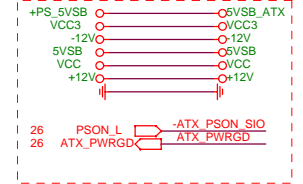


FRONT PANEL



POWER CONNECTOR

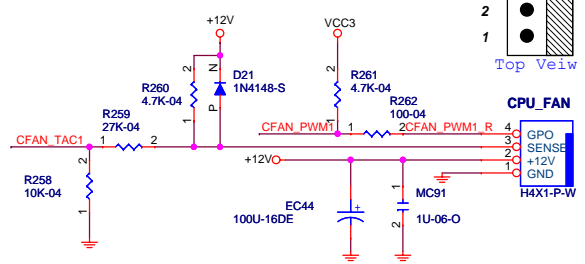
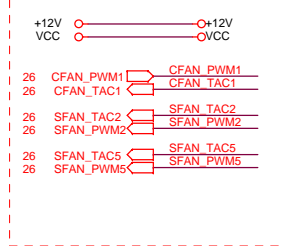
External Connection



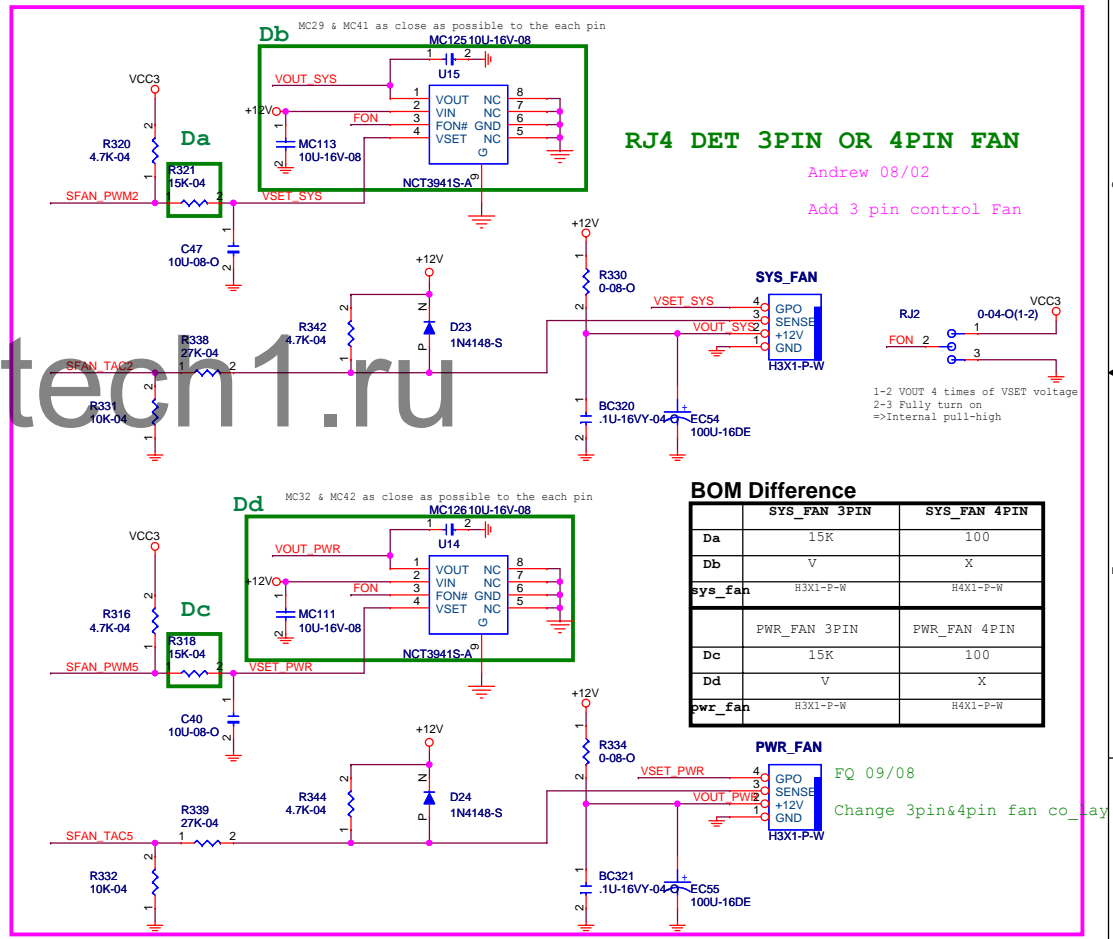
FAN

Kent 1016

External Connection

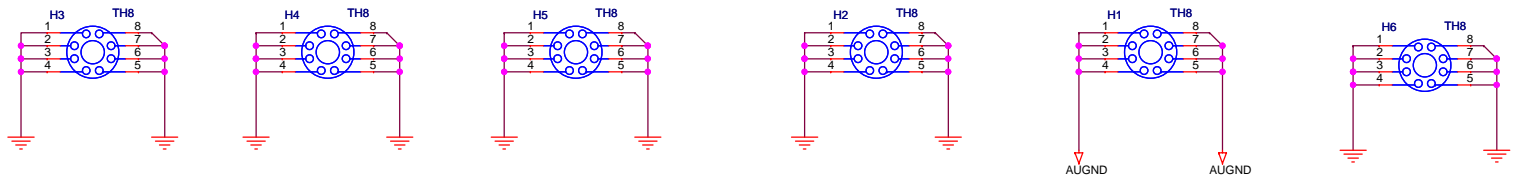


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BOM Difference

	SYS_FAN 3PIN	SYS_FAN 4PIN
Da	15K	100
Db	V	X
sys_fan	H3X1-P-W	H4X1-P-W
	PWR_FAN 3PIN	PWR_FAN 4PIN
Dc	15K	100
Dd	V	X
pwr_fan	H3X1-P-W	H4X1-P-W



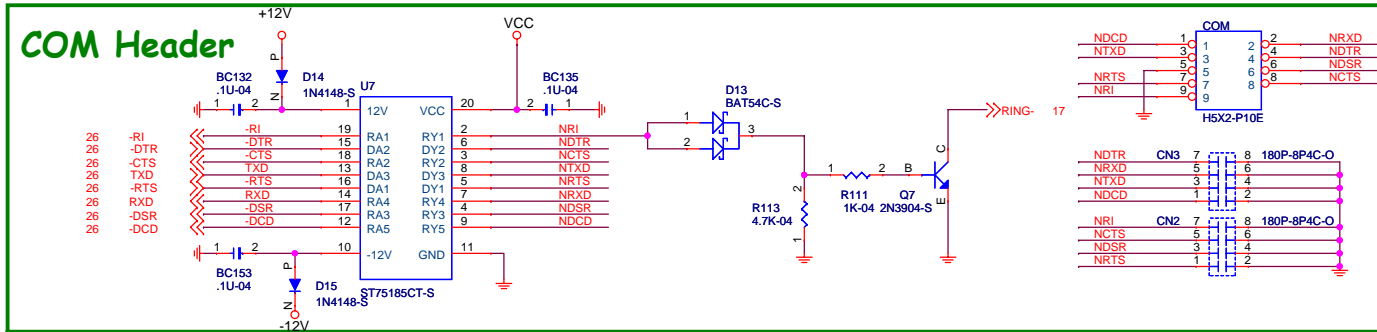
Elitegroup Computer Systems

F\_PANEL / FAN / PWR CONN

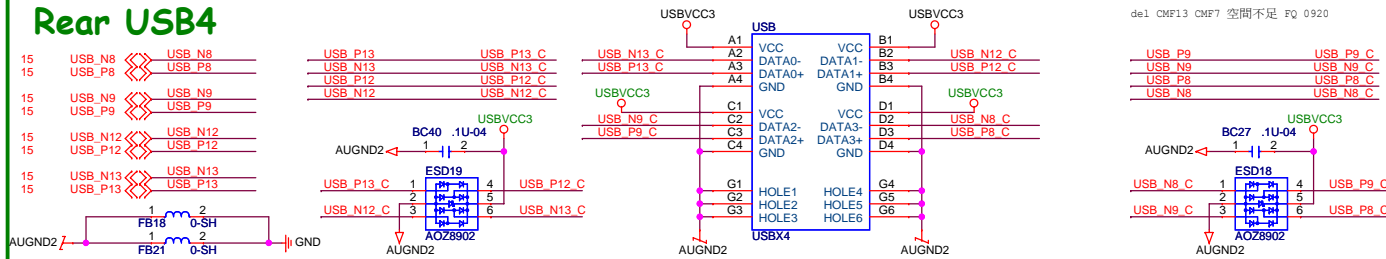
Size Custom Document Number H77H2-M4 Rev 1.0

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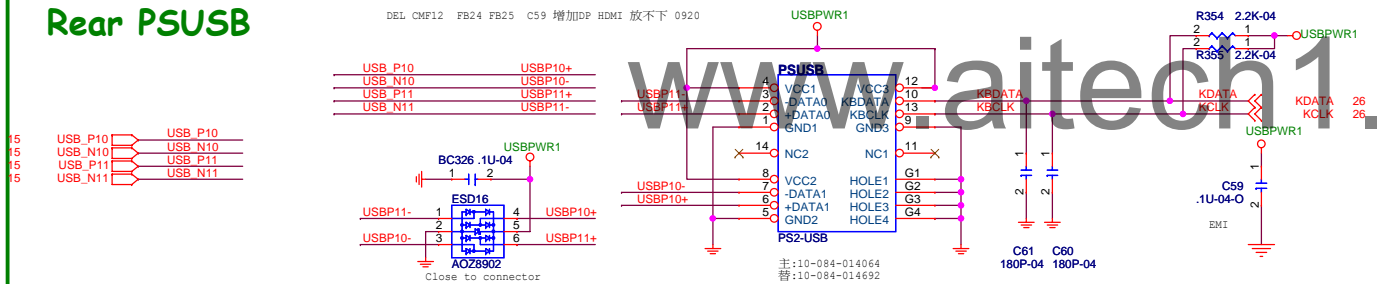
## COM Header



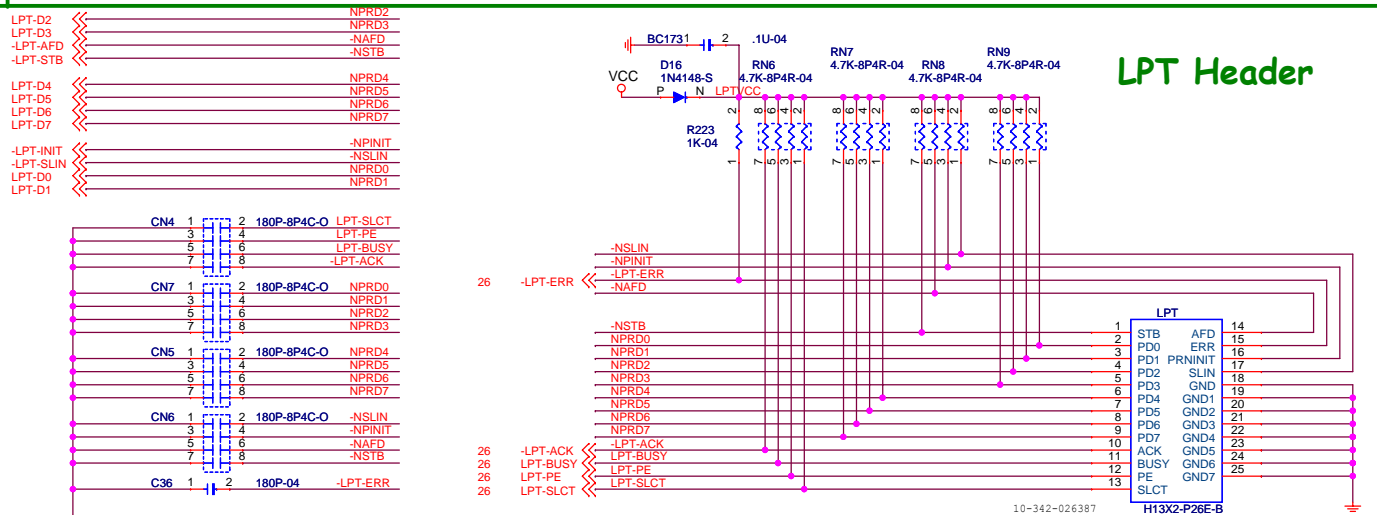
## Rear USB4



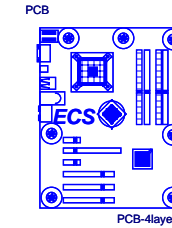
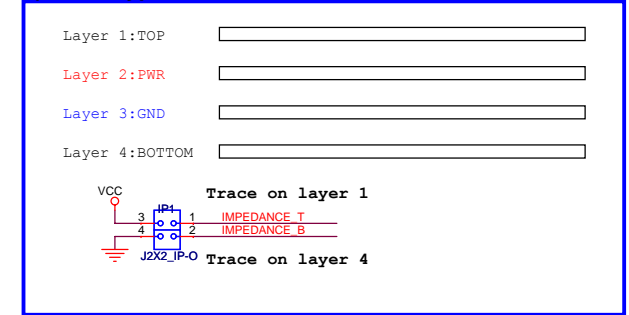
## Rear PSUSB



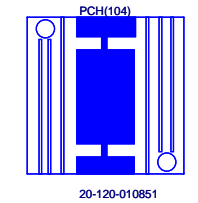
## LPT Header



## 1)Circuit type 1



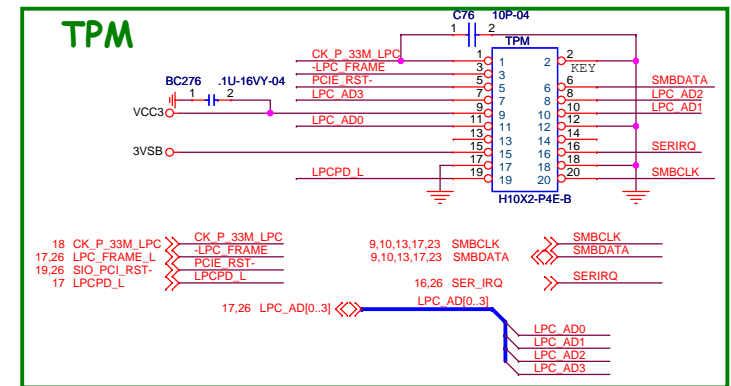
PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

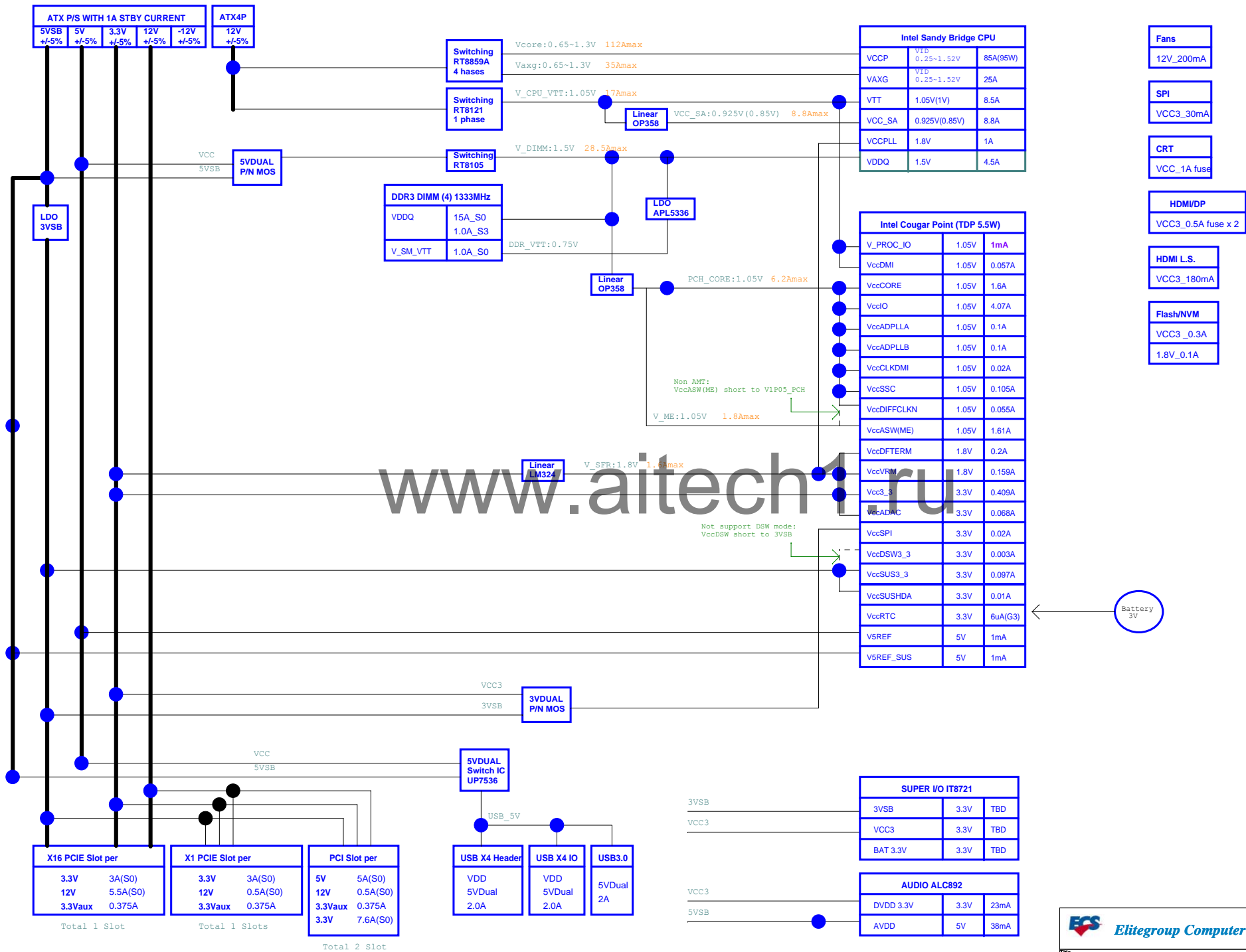


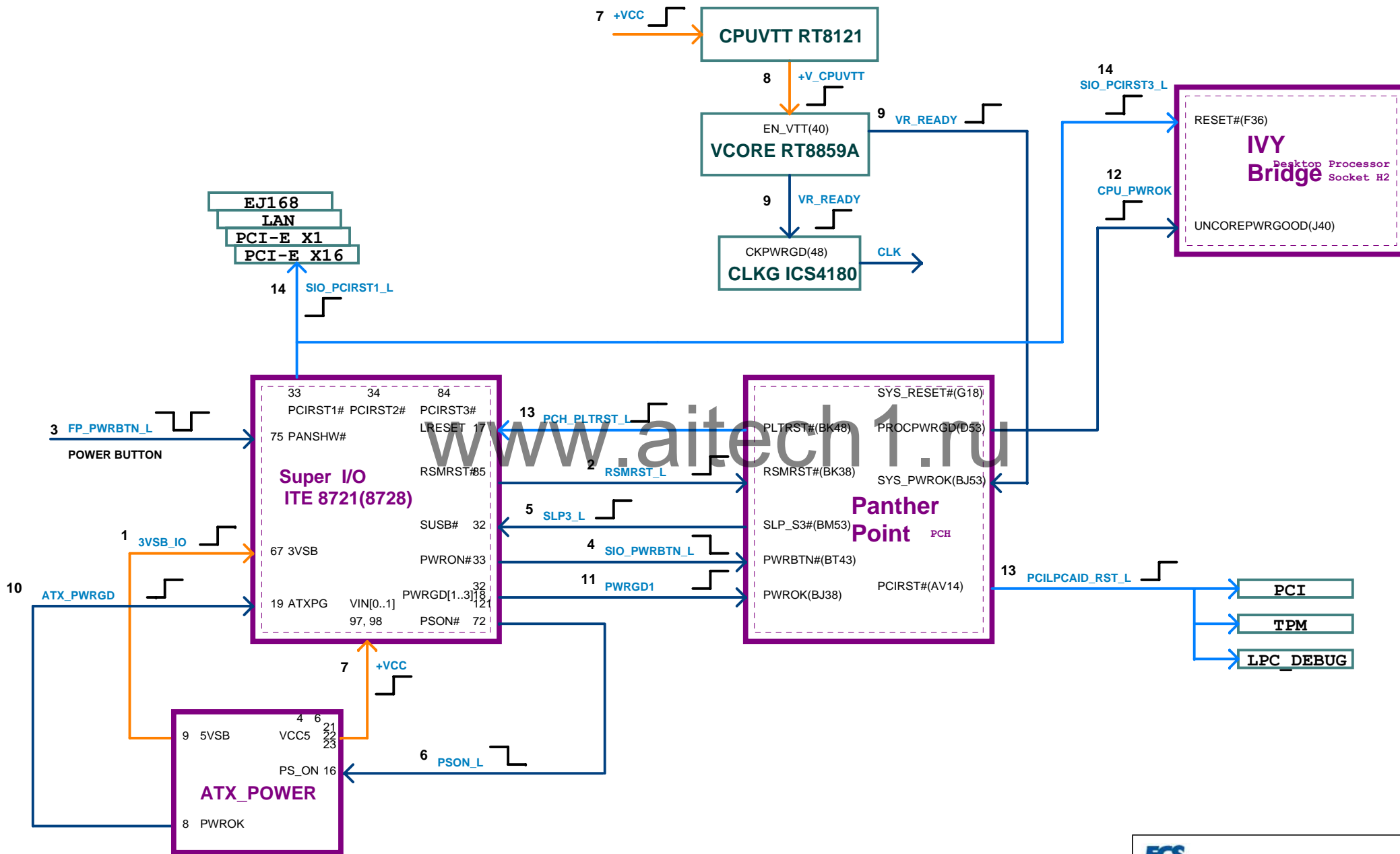
PN:20-120-010851



## TPM







**NOTE:**

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

